

# UPGRADE

# TDR

LHCb  
VELO

VERTEX LO  
CATOR

A schematic diagram of the LHCb detector upgrade, showing the layout of the Vertex Locator (VELO) and the LHCb detector components. The diagram is enclosed in a large black circle. A smaller circle on the left contains a zoomed-in view of the VELO structure. The main diagram shows the VELO (red and yellow) and the LHCb detector components (green and blue) arranged in a cross-like pattern. A black arrow points from the zoomed-in view to the main diagram.

## Technical Design Report







# LHCb VELO Upgrade Technical Design Report

The LHCb Collaboration

## Abstract

The upgraded LHCb VELO silicon vertex detector is a lightweight hybrid pixel detector capable of 40 MHz readout at a luminosity of  $2 \times 10^{33} \text{ cm}^{-2} \text{ s}^{-1}$ . The track reconstruction speed and precision is enhanced relative to the current VELO detector even at the high occupancy conditions of the upgrade, due to the pixel geometry and a closest distance of approach to the LHC beams of just 5.1 mm for the first sensitive pixel. Cooling is provided by evaporative  $\text{CO}_2$  circulating in microchannel cooling substrates. The detector contains 41 million  $55 \mu\text{m} \times 55 \mu\text{m}$  pixels, read out by the custom developed VeloPix front end ASIC. The detector will start operation together with the rest of the upgraded LHCb experiment after the LHC LS2 shutdown, currently scheduled to end in 2019. This Technical Design Report describes the upgraded VELO system, planned construction and installation, and gives an overview of the expected detector performance.



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# Contents

<b>1</b>	<b>Introduction</b>	<b>1</b>
1.1	Current system overview . . . . .	2
1.2	LHCb upgrade beam conditions . . . . .	4
1.3	VELO upgrade overview . . . . .	5
<b>2</b>	<b>Requirements</b>	<b>9</b>
2.1	Irradiation constraints . . . . .	9
2.2	Geometry constraints . . . . .	10
2.3	Data rate constraints . . . . .	14
2.4	Mechanical constraints . . . . .	14
2.5	Machine interface and VELO aperture . . . . .	16
2.6	Physics performance constraints . . . . .	17
<b>3</b>	<b>Layout overview</b>	<b>19</b>
3.1	Geometry in simulation . . . . .	19
3.1.1	Modules . . . . .	19
3.1.2	RF foil . . . . .	21
3.1.3	$z$ layout . . . . .	21
3.2	Material scan . . . . .	23
<b>4</b>	<b>Performance</b>	<b>27</b>
4.1	Occupancy . . . . .	27
4.2	Hit resolution . . . . .	28
4.3	Track reconstruction . . . . .	29
4.3.1	Reconstruction efficiency . . . . .	29
4.3.2	Hit efficiency . . . . .	32
4.3.3	Timing . . . . .	34
4.4	Primary vertex and impact parameter resolutions . . . . .	35
4.5	Decay time resolution . . . . .	40
4.6	Performance after irradiation . . . . .	42
<b>5</b>	<b>Module</b>	<b>46</b>
5.1	Module specifications, design considerations and layout . . . . .	46
5.2	Sensors . . . . .	46
5.3	Tile production . . . . .	53
5.4	Hybrid and additional on-board electronics . . . . .	54
5.5	Module pedestal . . . . .	56
5.6	Module assembly procedures and quality assurance . . . . .	58

<b>6</b>	<b>VeloPix</b>	<b>60</b>
6.1	Overview . . . . .	60
6.2	Specifications . . . . .	60
6.3	Architecture . . . . .	63
6.3.1	Global architecture . . . . .	63
6.3.2	Front-end analog and digital . . . . .	63
6.3.3	Super-pixel concept . . . . .	65
6.3.4	End of column logic . . . . .	65
6.3.5	Fast serialisers . . . . .	67
6.3.6	TFC and ECS interface . . . . .	67
6.4	Design and simulation . . . . .	68
6.5	Prototyping . . . . .	70
<b>7</b>	<b>Electronics</b>	<b>72</b>
7.1	System Architecture . . . . .	72
7.2	Front-end hybrids . . . . .	72
7.2.1	Construction . . . . .	72
7.2.2	Electrical functionality . . . . .	74
7.3	Electrical high speed cables . . . . .	74
7.3.1	Number of signals . . . . .	75
7.3.2	Cable construction . . . . .	75
7.3.3	Signal integrity . . . . .	75
7.3.4	Connectors . . . . .	76
7.3.5	Vacuum feedthroughs . . . . .	76
7.4	Opto and power board . . . . .	77
7.5	Power supplies . . . . .	78
7.6	Detector grounding scheme . . . . .	79
7.7	Interlock system . . . . .	79
7.8	Radiation qualification . . . . .	79
7.9	Prototyping . . . . .	80
7.9.1	Electrical high speed cable prototypes . . . . .	80
7.9.2	OPB prototyping . . . . .	81
7.9.3	DC/DC tests . . . . .	81
<b>8</b>	<b>VELO DAQ integration</b>	<b>82</b>
8.1	VELO firmware and software, ECS . . . . .	82
8.2	VELO DAQ slice development . . . . .	84
<b>9</b>	<b>Cooling</b>	<b>85</b>
9.1	Requirements . . . . .	85
9.2	Microchannel cooling solution . . . . .	86
9.3	Microchannel cooling R&D . . . . .	87
9.4	Thermal mockup of a pixel module . . . . .	90

9.5	Channel dimensions and layout . . . . .	92
9.6	Connector Design . . . . .	94
9.7	Cooling system architecture . . . . .	96
9.8	Cooling system safety . . . . .	97
<b>10</b>	<b>Mechanics</b>	<b>98</b>
10.1	RF foil . . . . .	99
10.1.1	Manufacturing technique and prototypes . . . . .	100
10.2	Detector base and hood . . . . .	102
10.2.1	Base . . . . .	102
10.2.2	Hood . . . . .	103
10.2.3	Feedthroughs . . . . .	103
10.3	Assembly and transport . . . . .	104
10.3.1	Assembly method . . . . .	104
10.3.2	Transport . . . . .	105
10.3.3	Reception . . . . .	106
10.4	Installation sequence . . . . .	106
10.5	Vacuum and motion control systems . . . . .	106
10.6	Timeline for mechanics . . . . .	107
10.7	Safety . . . . .	107
<b>11</b>	<b>Project organisation</b>	<b>108</b>
11.1	Participating institutes and responsibilities . . . . .	108
11.2	Schedule . . . . .	109
11.3	Cost, resources and contingencies . . . . .	113
<b>12</b>	<b>Acknowledgements</b>	<b>117</b>
	<b>References</b>	<b>117</b>



# 1 Introduction

This Technical Design Report (TDR) describes the planned upgrade of the currently installed VErteX LOcator (VELO), the silicon vertex detector that surrounds the interaction region at LHCb [1]. The existing detector will be replaced with a pixel detector capable of 40 MHz readout, featuring modules with integrated microchannel evaporative CO<sub>2</sub> cooling. This upgrade forms part of the global upgrade of the LHCb experiment, which is currently scheduled to start data taking in 2019, after the second long shutdown (LS2) of the LHC.

The principal task of the VELO is to enable LHCb to trigger on and reconstruct displaced vertices, as well as playing a significant role in the tracking. It must cover the full momentum and angular range of the LHCb detector. Due to the fact that it surrounds the interaction region the VELO adds partial information for tracks falling outside this acceptance, in particular in the backwards direction. The currently installed VELO also includes two stations in the backwards direction capable of 40 MHz readout. These “Pile-Up” stations provide information for the luminosity analyses and play a role in the L0 trigger. The information from the VELO is critical to identify characteristic displaced vertices of heavy flavoured particles, underpinning physics analyses within LHCb. At trigger level the VELO identifies tracks with high impact parameter and is the first handle to reduce the minimum bias rate. The offline performance of the VELO is equally important. The excellent secondary vertex resolution is vital to resolve  $B_s^0$  meson oscillations and to allow time dependent CP violation analyses. The impact parameter resolution must remain precise at both trigger and offline stages even at the relatively low transverse momentum regimes of the daughter products of  $b$ - and  $c$ -hadrons, and the detector must be fully efficient in order to capture multi-body final hadronic states.

The current LHCb experiment has been re-optimised and is now able to accumulate data at a typical luminosity of  $4 \times 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$ , about twice the original design luminosity. It is expected to have accumulated an integrated luminosity of the order of  $8 \text{ fb}^{-1}$  by the start of LS2. When LHC running resumes after LS2 the LHCb collaboration wishes to increase the number of collected  $b$ -hadron decays by a factor 10 – 20 in a reasonable time span. In order to access higher luminosities an upgrade of the entire experiment is needed, in combination with an improved trigger scheme. The current first level hardware trigger reduces the rate from 40 to 1 MHz. This means that when running at higher luminosities it would be necessary to increase the trigger thresholds at constant bandwidth with consequent loss of hadronic  $B$  decays.

At the upgrade the hardware trigger will be replaced by a triggerless system with output rates of up to 40 MHz. Data will be sent to a large CPU farm where a flexible software trigger, with access to full event information, will operate. In addition to the modification of all subdetector electronics to comply with this scheme, changes need to be made to the detector to allow for more complex pattern recognition requirements in high pile-up environment and cope with a higher integrated radiation dose. The upgraded detector is expected to be capable of accumulating  $50 \text{ fb}^{-1}$ , and all the LHCb upgrade subdetectors including the VELO must be qualified in performance up to a luminosity of  $2 \times 10^{33} \text{ cm}^{-2} \text{ s}^{-1}$ , to allow evolutions of the trigger beyond the initially envisaged

$1 \times 10^{33} \text{ cm}^{-2} \text{ s}^{-1}$ . As for the current VELO, there is an emphasis on the reconstruction of the decay products of beauty and charm hadrons, so the low transverse momentum range plays a critical role and the minimisation of material in the VELO is crucial.

The concept of the upgraded VELO has been previously outlined in the LHCb Upgrade Letter of Intent (LoI [2]) and LHCb Upgrade Framework TDR (FTDR [3]). Since that time the design has considerably evolved, as described in this TDR. Some of the major developments are as follows:

- The option of microchannel cooled hybrid pixel modules has been made following an internally and externally refereed review;
- The understanding of the digital architecture of the readout chip has matured, and the choice has been made for a binary readout;
- There has been a full implementation of a realistic pixel geometry in the simulation, and the module layout and foil shape have been reoptimised;
- The microchannel cooling technology has been shown to withstand high pressures, and endurance testing has begun.

There are technical design choices which remain to be taken, among which we highlight the choice of vendor and substrate type for the sensor technology, the detailed cooling plant design, and the technology choice for the vacuum feedthroughs. In this document, where it has been possible or necessary, the figures and results are shown with the latest layout and module design. For figures and studies which are not sensitive to these details, or for which the software has not yet been fully tuned, results are shown with the LoI layout and potential changes are discussed.

This document is organised as follows. The system is introduced, and the requirements laid out in the following two sections. The layout and expected physics performance of the upgraded detector is described in Sect. 3 and Sect. 4. The pixel module is described in Sect. 5 and the following sections are devoted to the ASIC, electronics, cooling, data acquisition (DAQ) integration and mechanics. Finally in Sect. 11 the project schedule and organisation are described.

## 1.1 Current system overview

The currently installed VELO is manufactured with 84 single-sided radial ( $R$ ) and azimuthal-angle ( $\phi$ ) measuring strip sensors operated in a secondary vacuum inside the LHC beam pipe. The  $R$  and  $\phi$  sensors are mounted on either side of a highly thermally conductive spine which also supports the readout hybrid, and the resulting double sided module is supported on a carbon fibre paddle stand. The modules are arranged perpendicularly to the beam along a length of about 1 m. Module cooling is provided by evaporative  $\text{CO}_2$  circulating in stainless steel pipes embedded within aluminium pads which are clamped to the base of the module. The detector is divided into two moveable

halves, allowing it to retract during LHC injection. The cabling between the modules and detector hood must be flexible enough to absorb these movements, which occur for every LHC fill. The modules are separated from the primary vacuum with a 300  $\mu\text{m}$  thin aluminium foil (RF foil). In the beam pipe region the material is corrugated in such a manner as to reduce as much as possible the material traversed by particles before their first measured point. Additional corrugations are provided in order to allow the two sides of the VELO to close completely, ensuring full geometrical coverage. A small overlap is added for alignment purposes. For more details see [1].

The arrangement of the array of VELO modules within the vacuum tank is shown in Fig. 1. The vacuum tank and stand, which together represent a significant fraction of effort and investment in the construction of the current VELO, can be reused for the upgrade, along with the rectangular bellows which allow the movement of the two halves. The RF foil and detector support and hood will be modified to be compatible with upgrade requirements, as described in Sect. 10. The very successful mixed phase  $\text{CO}_2$  cooling system will also be reused for the upgrade, however with considerable modifications.

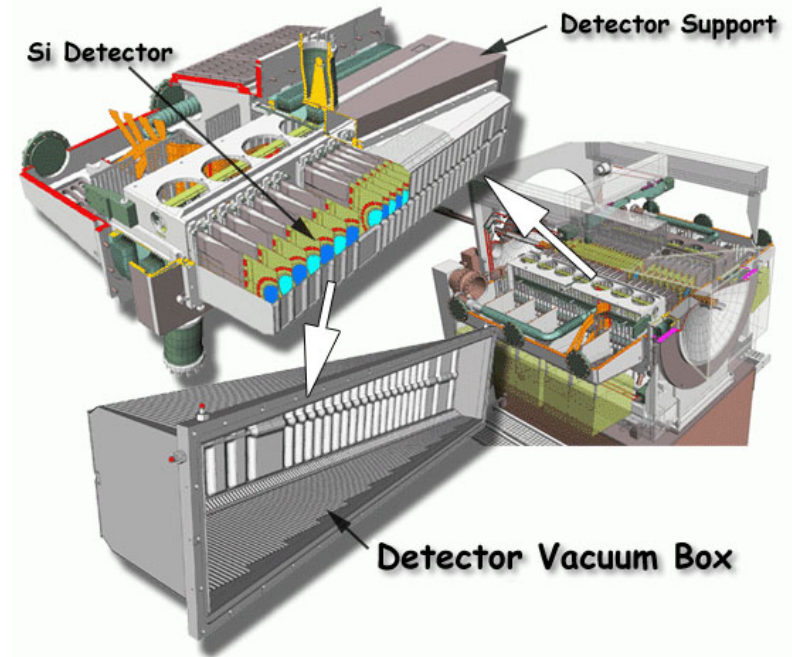


Figure 1: Layout overview of the current VELO, illustrating the vacuum tank, module positioning and RF foil. For the upgrade it will be necessary to change the modules, foil, module bases, and detector hoods, in addition to major refurbishment of the motion, vacuum and cooling system.

Table 1: Overview of global upgrade settings for simulation.

Beam energy	7 TeV
Number of bunches colliding at IP8	2400
Bunch $z$ RMS	90 mm
Half angle horizontal	135 $\mu$ rad
Half angle vertical	120 $\mu$ rad
Luminosity	$2 \times 10^{33} \text{ cm}^{-2} \text{ s}^{-1}$
Bunch charge	$1.2 \times 10^{11}$ protons
$\nu$ (# interactions per crossing)	7.6 (for $\sigma_{\text{tot}} = 102.5 \text{ mb}$ )
$\mu$ (# visible interactions per crossing)	5.2 (for $\sigma_{\text{vis}} = 70.6 \text{ mb}$ )
Bunch $x,y$ RMS	37.70 $\mu$ m
$z$ RMS luminous region $\sigma_{\text{lumi}}$	63 mm

## 1.2 LHCb upgrade beam conditions

All LHCb subdetectors at the upgrade will face increased occupancies and rates, due to the increase in luminosity and beam energy. The change to a 25 ns bunch spacing will be mandatory to avoid prohibitive occupancies in the tracking detectors. The current best estimates of the beam conditions at the upgrade, which have been used in the simulation studies, are given in Table 1. Of particular interest to the VELO are the  $z$  RMS of the beam and crossing angle, which together determine the extent of the luminous region in  $z$  in LHCb to be around  $\sigma_{\text{lumi}} = 63 \text{ mm}$ . This affects the number of stations which must be distributed around the interaction region, and also has an influence on the minimum aperture available at LHCb. Another important parameter is the number of bunches colliding at IP8, which has been put at a conservative 2400 bunches, whereas we hope in practice to achieve the maximum possible 2622 bunches, which will ease slightly the occupancy situation at LHCb. The VELO upgrade performance has been evaluated for these conditions, corresponding to  $\nu = 7.6$ , however in order to understand the robustness and to take into account the possibility of less favourable filling schemes, larger multiplicities than expected, and increased numbers of secondaries the behaviour has been explored for higher data rates and number of primary vertices.

The evolution of the interaction rates as the luminosity increases is shown on the left side of Fig. 2, while the right side of the figure shows the mean number of vertices per visible event in LHCb<sup>1</sup>. Note that the rates displayed here are an average, and the instantaneous rate can be as high as 40 MHz, which is the peak value used in the estimation of data rates. The expected distribution of the number of vertices per event visible in LHCb is shown in Fig. 3. At the upgrade ( $\mu \sim 5.2$ ) the number of empty events is almost eliminated, in contrast to the situation in current running ( $\mu \sim 1.7$ ).

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<sup>1</sup>defined as  $\mu/(1 - e^{-\mu})$ .



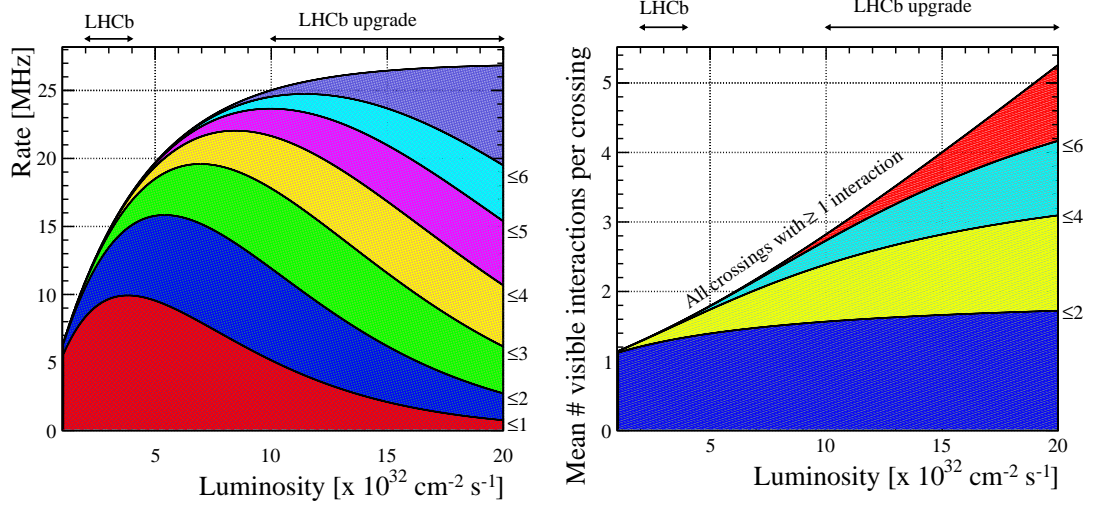


Figure 2: (left) Evolution of interaction rates in LHCb (for 25 ns running, as will be the case after LS1) as a function of luminosity, split into categories of number of interactions per event. A significant increase in pile-up is visible when going from  $1$  to  $2 \times 10^{33} \text{ cm}^{-2} \text{ s}^{-1}$ . (right) Average number of  $pp$  interactions per bunch crossing visible in LHCb as a function of luminosity, for events with at least one visible interaction.

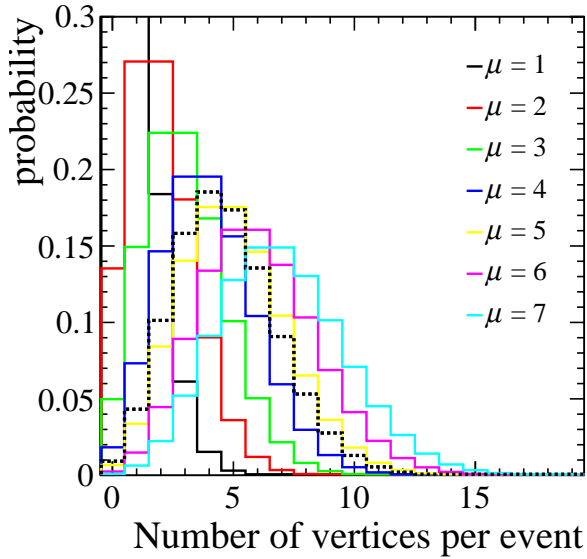


Figure 3: Number of vertices per event for running at various values of  $\mu$ . The default value used in the simulation, corresponding to  $2 \times 10^{33} \text{ cm}^{-2} \text{ s}^{-1}$ , is indicated by the dotted line.

### 1.3 VELO upgrade overview

As explained above, the upgraded VELO must maintain or improve its physics performance while delivering readout at 40 MHz in the operating conditions of the upgrade. This can only be achieved by a complete replacement of the silicon sensors and electronics. Following an externally refereed review the collaboration has chosen to install a detector

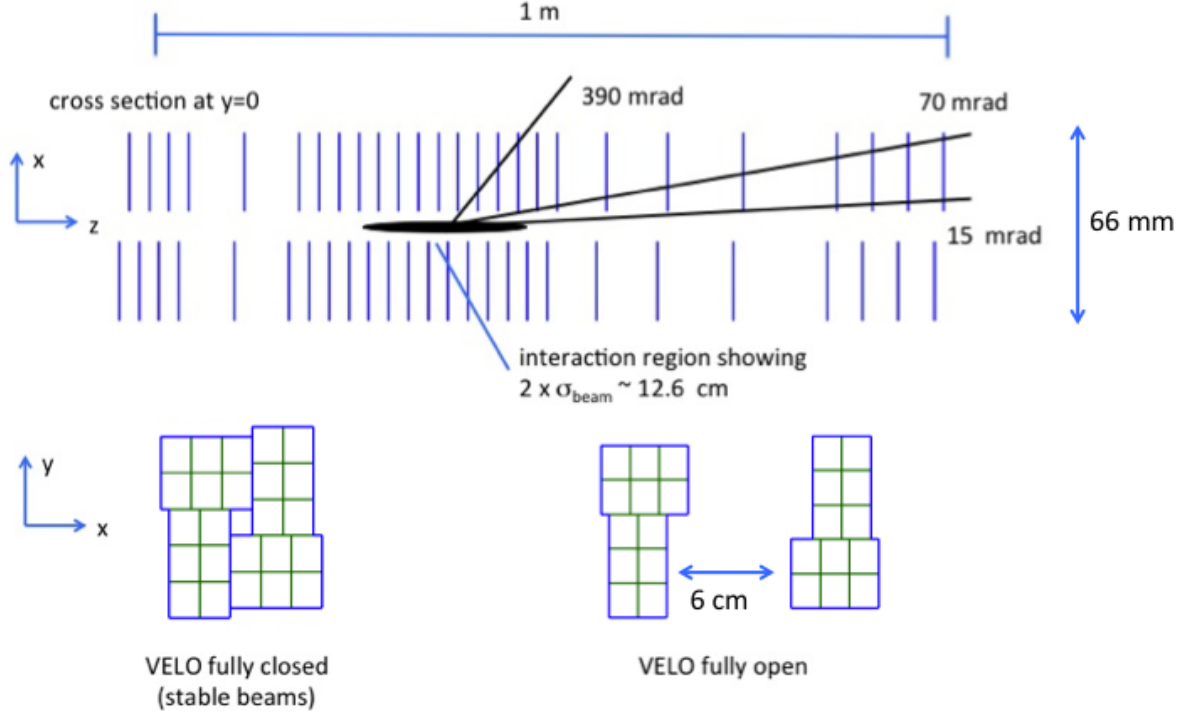


Figure 4: Schematic layout of the upgraded VELO.

based on hybrid pixel sensors. A new radiation hard ASIC, dubbed VeloPix, capable of coping with the data rates, is under development. The module cooling design must be upgraded in order to protect the tip of the silicon from thermal runaway effects after significant irradiation, and to cope with the high speed pixel ASIC power dissipation. For this reason the upgrade cooling is integrated within the module, in contrast to the currently installed detector. The cooling is provided by evaporative  $\text{CO}_2$  circulating within miniature channels etched into thin silicon substrates which form the backbone of the modules. The upgraded VELO reuses large parts of the current mechanical infrastructure, in particular the vacuum tank, and elements of the very successful mixed phase  $\text{CO}_2$  cooling system.

The conceptual layout of the detector within the LHCb coordinate system is shown in Fig. 4. It is very similar to the current VELO layout, however the  $z$  positions of the modules have been changed in order to reach similar acceptance given the smaller module size and smaller distance from the beam line to the first measured point. The detailed optimisation procedure is described in Sect. 3.1.3. The positions of the modules in the

closed (LHC stable beam operation) and open position are also shown. Note that in contrast to the current VELO no additional overlap is needed as due to the non projective L-shape geometry approximately 10% of tracks traverse both the left and right side, and can be used to align the sides.

In the following some VELO-specific terms are defined, which are used throughout this document.

- **Tiles** are assemblies of three VeloPix ASICs in a row bump-bonded to a common silicon sensor.
- The printed circuit boards which are mounted on both sides of a module and provide electronic support for the front-end ASICs and the bias voltage for the sensors are known as **hybrids**.
- The VELO consists of an array of **modules** which comprise the tiles and associated services (cooling and readout) inside the vacuum. Each module comprises two hybrids.
- The term **station** (used primarily in tracking) refers to a pair of modules. The  $i$ -th station comprises the  $i$ -th module in the left half and the  $i$ -th module in the right half.
- The left half (A side) is at positive  $x$ , the right half (C side) is at negative  $x$ .

The sensor tiles and modules are described in Sect. 5. As for the current VELO it is important to optimise the material throughout the module, including the sensor, hybrid and base regions, since all elements fall at least partially within the detector acceptance, as illustrated in Fig. 5. The L shape pixel module has major implications for the RF foil, which must change its shape to match the module edge, making the previous construction technique impossible. A new approach has been taken to the foil production, which is described in Sect. 10. An artist's impression of the upgraded VELO installed within the vacuum tank is shown in Fig. 6.

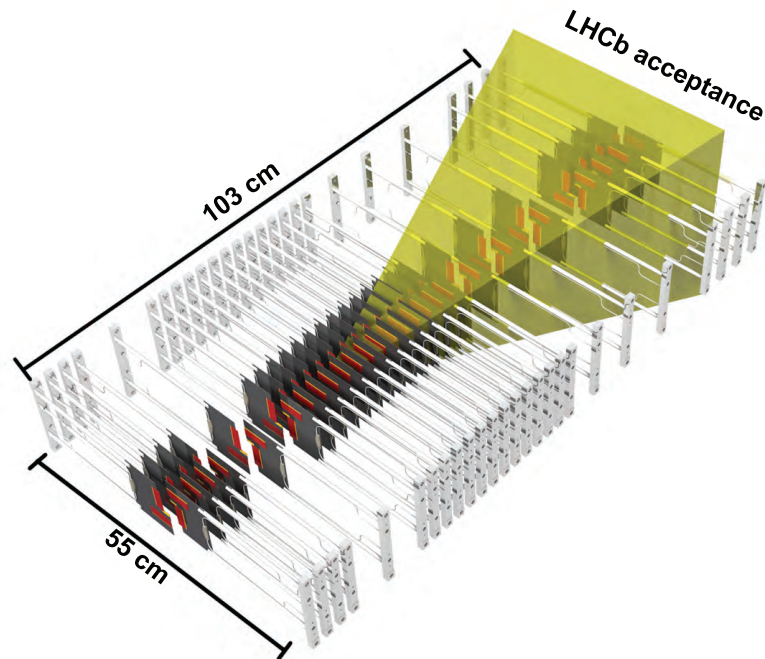


Figure 5: Upgrade VELO module layout, with the LHCb acceptance shaded. This figure illustrates how various parts of the modules fall into the acceptance of physics quality tracks.

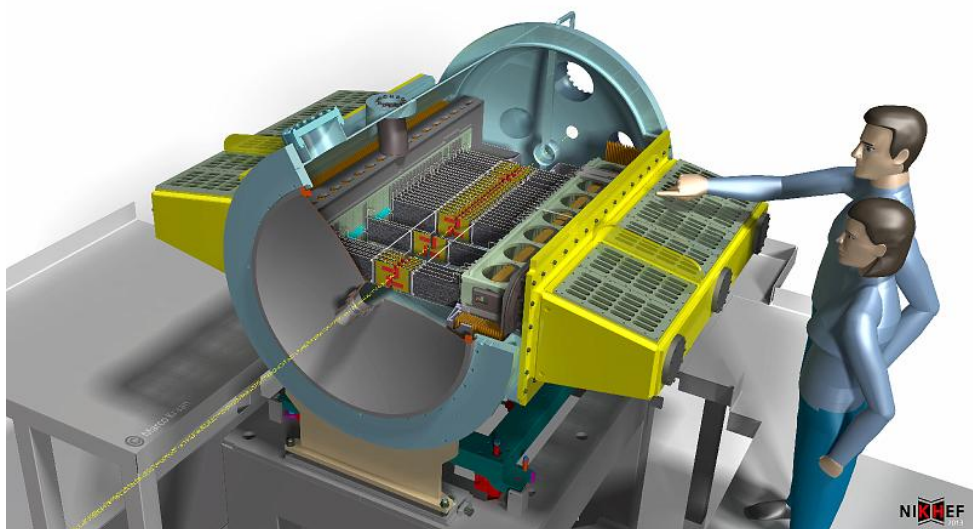


Figure 6: Artist's impression of the upgraded VELO once installed.

## 2 Requirements

The design of the VELO upgrade satisfies a set of performance criteria, in addition to the necessity for the system to survive an integrated luminosity of  $50 \text{ fb}^{-1}$  at upgrade conditions. This section introduces the major issues which affect the design and performance.

### 2.1 Irradiation constraints

The current VELO is designed to withstand an integrated luminosity of around  $10 \text{ fb}^{-1}$ . After this time the signal-to-noise ratio is expected to decrease below the performance limit and the current temperature drop of about  $19^\circ\text{C}$  between the  $\text{CO}_2$  cooling channel and the silicon tip is expected to be insufficient to protect the module from going into thermal runaway.

The expected flux at the upgrade has been studied in simulation in the beam conditions given above. The method used is similar to that used to estimate radiation damage in the current VELO, which has so far given a very reliable prediction of the measured sensor leakage currents [4], as illustrated in Fig. 7.

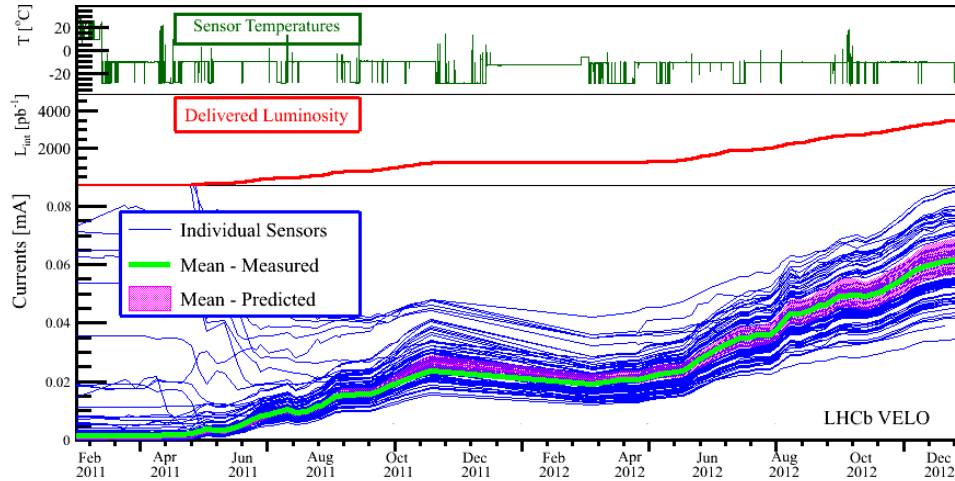


Figure 7: Radiation damage as measured by sensor leakage currents in the presently installed VELO, compared to the prediction obtained from a study of simulated occupancies. The large spread of currents due to sensor positions can be seen, as well as a good agreement between the predicted and measured currents. These results give a good measure of confidence in the estimates for rates in upgrade conditions.

The expected radiation damage at the upgrade is shown in Figs. 8 and 9. Figure 8 shows fluence contours in the  $R - z$  plane. The vertical axis has been set to a logarithmic scale to enhance the visibility of the high-dose region, and the vertical lines mark the  $z$  positions where the modules will be mounted. The region which receives the highest

dose is concentrated at low radius and around the interaction region. Note that for good impact parameter resolution this is the region where the measurements make the most important contribution.

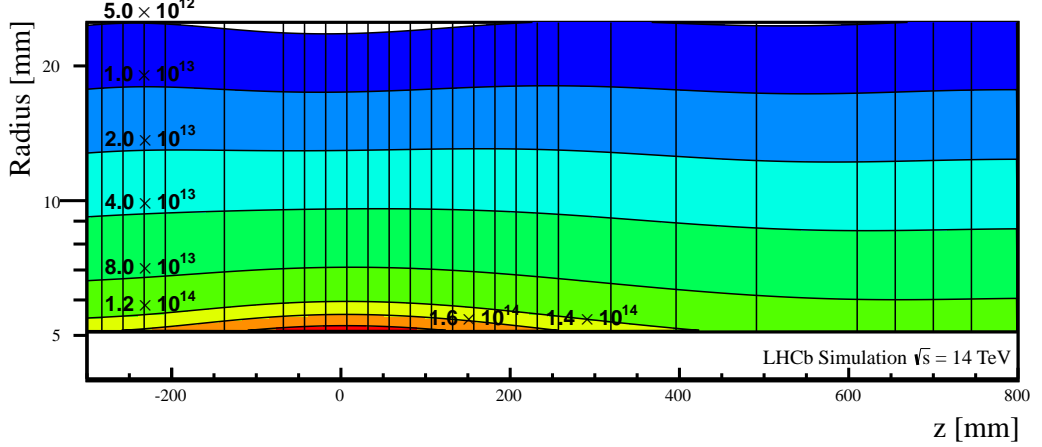


Figure 8: Estimated integrated radiation dose in the  $R - z$  plane per  $\text{fb}^{-1}$  at upgrade conditions expressed in units of  $1 \text{ MeV n}_{\text{eq}}/\text{cm}^2$ . The radiation damage contours are shown. Note that the vertical axis is logarithmic, in order to highlight the behaviour around the interaction region.

Figure 9 shows the fluence as a function of radius for the most highly irradiated and most distant, downstream sensor. The fluence has an exponential shape per sensor, with the greatest dose experienced above the interaction region, and a factor two reduction in downstream stations. The curves are fitted with the expression  $A \times R^{-k}$ , where  $R$  is the radius in cm, and the  $A$  and  $k$  fitted constants are shown as a function of  $z$  position.

The upgraded detector is expected to accumulate a maximum integrated flux of up to  $\sim 8 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$ . After this dose one expects currents of approximately  $200 \mu\text{A}/\text{cm}^2$  at  $-20^\circ\text{C}$  at a bias voltage of 1000 V at the position of the closest pixel, equivalent to roughly 7 nA for  $55 \times 55 \mu\text{m}^2$  square pixels. At these doses and currents, the most challenging issue will be protecting the silicon tip from thermal runaway, without introducing too much material into the acceptance. The electronics will be required to be sufficiently radiation hard and single-event-upset (SEU) tolerant.

## 2.2 Geometry constraints

As illustrated in Fig. 10 tracks originating from secondary vertices with large impact parameters are the principal signature of beauty and charm hadrons decaying in LHCb. The trigger algorithms of LHCb in both the current detector and the upgrade rely on an impact parameter cut, hence the impact parameter resolution is an excellent benchmark performance number for the detector. Due to the forward geometry of LHCb, the sensor  $z$  resolution plays a minor role and the three-dimensional impact parameter resolution is given by the sum in quadrature of the individual  $x$  and  $y$  impact parameter resolutions,

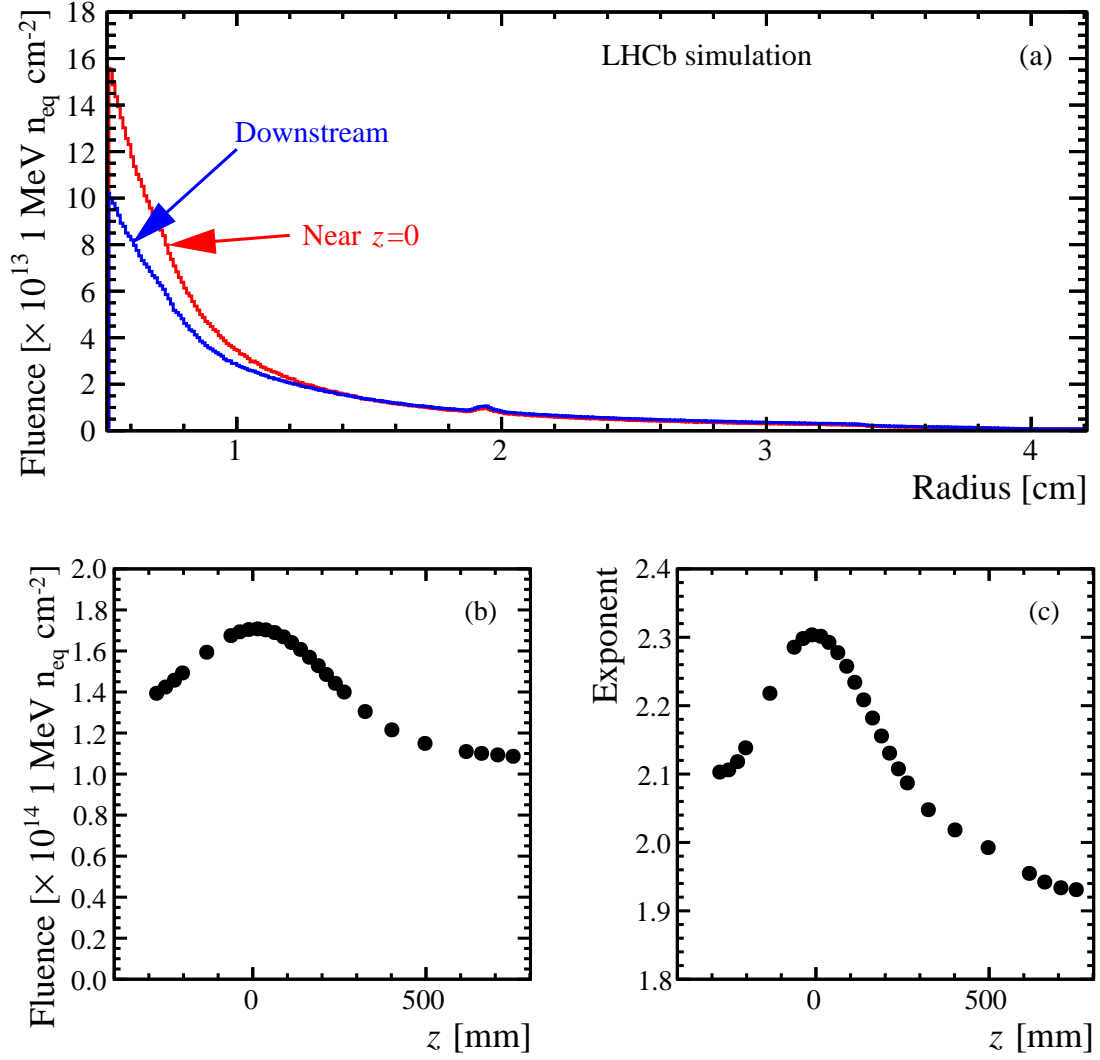


Figure 9: (a) Fluence as a function of radius  $R$  per delivered  $\text{fb}^{-1}$  for the most highly irradiated sensor (above interaction region) and the sensor receiving the smallest dose (downstream). The shape for each sensor is fitted with the expression  $A \times R^{-k}$ , where  $R$  is the radius in cm and the  $A$  and  $k$  are fitted constants. (b) shows the dose measured at the position of the closest pixel as a function of  $z$  position, and (c) shows the value of the exponent  $k$ , showing how the radiation map flattens further away from the interaction region.

with the relation  $\sigma_{3D} = \sqrt{\frac{\pi}{2}} \sigma_{\text{IP}}$ , where  $\sigma_{\text{IP}}$  is the RMS of either the  $x$  or  $y$  impact parameter component.

Under the assumption that the amount of material at the first measured point is reasonably compact, the impact parameter resolution is well described to first order by the following expression:



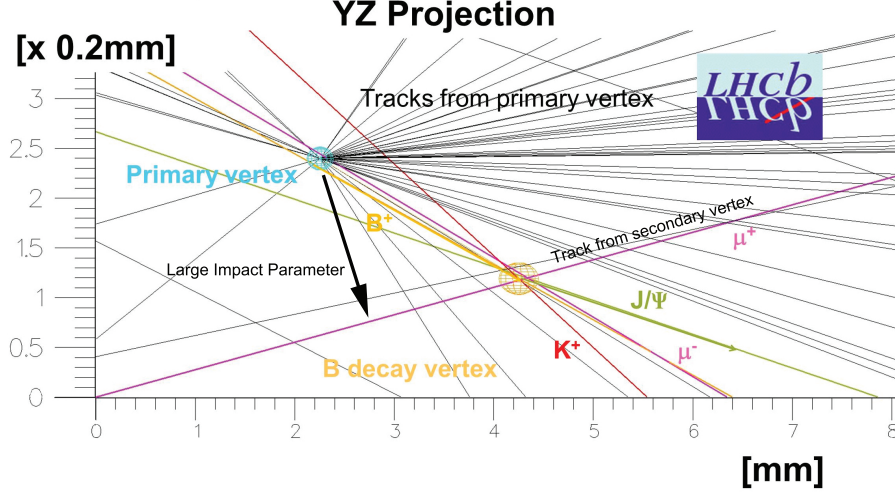


Figure 10: Signature of  $B$  decay products from a  $B^+ \rightarrow J/\psi K^+$  candidate event in LHCb data.

$$\begin{aligned} \sigma_{\text{IP}}^2 &= \frac{r_1^2}{p_T^2} \left( 0.0136 \text{ GeV}/c \sqrt{\frac{x}{X_0}} \left( 1 + 0.038 \ln\left(\frac{x}{X_0}\right) \right) \right)^2 + \frac{\Delta_{02}^2 \sigma_1^2 + \Delta_{01}^2 \sigma_2^2}{\Delta_{12}^2} \\ &= \sigma_{\text{MS}}^2 + \sigma_{\text{extrap}}^2. \end{aligned} \quad (1)$$

In this formula  $r_1$  is the radius of the first measured point on the track;  $p_T$  is the transverse momentum of the track;  $x/X_0$  is the fractional radiation length before the second measured point, which includes the foil, any dead area of silicon traversed, and the material of the first measured point;  $\sigma_1$  and  $\sigma_2$  are the measurement errors on the first and second point, respectively; and  $\Delta_{ij}$  represents the distance between  $i$  and  $j$ , where  $i$  and  $j$  can be 0 (the vertex), 1 (the first measured point), or 2 (the second measured point).

This formula gives an indication of the driving factors behind the design. The presence of the  $r_1^2$  term indicates that the first measured point should be as close to the interaction point as possible, which is achieved by designing the minimum possible inner dimensions, reducing the size of the guard rings, and having as many stations as possible. The presence of the  $\sqrt{x/X_0}$  term shows on the other hand, the importance of reducing the number of stations, of having the stations as thin as possible, and of reducing the material contribution of the RF foil which encapsulates the detector secondary vacuum volume. The effect of this material term on the impact parameter resolution as a function of transverse momentum is illustrated, for the current VELO, in Fig. 12, discussed below. The final term in Eq. 1 illustrates the importance, for high momentum tracks, of maintaining the best possible precision. Additional considerations enter the design, in particular the importance of having stations surrounding the interaction region including the negative  $z$  side for reconstruction of backward tracks, in order to measure the primary vertices as accurately



as possible, and the overall performance of the detector in terms of the trigger algorithm and the time taken to implement this algorithm in the computer farm.

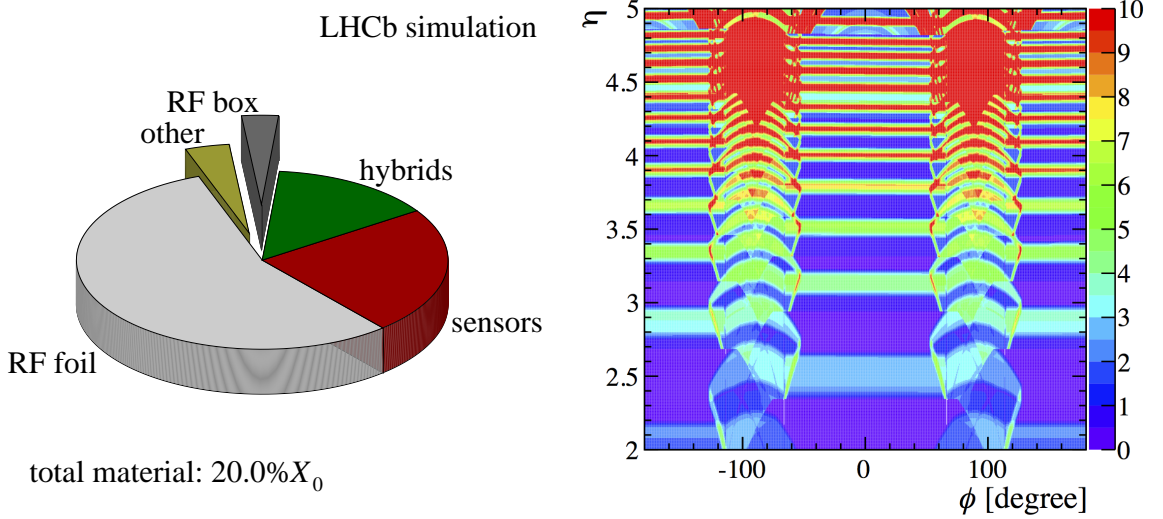


Figure 11: The pie chart shows a breakdown of the total material of the currently installed VELO by component. The largest contribution comes from the RF foil; this is expected to also be a very significant component at the upgrade. The right figure shows a scan in the  $\eta$ - $\phi$  plane of the amount of material (in percentage of a radiation length) seen by tracks before the first measured point in the VELO. The horizontal lines are due to the sensor planes and the spiral shapes come from the material structure in the overlap region. Note that particles frequently cross the foil multiple times before the first measured point, and may also pass through the guard ring insensitive part of a module before eventually registering a hit in the next station. The average material before the first measured point is  $\sim 4.6\% X_0$ . For a comparison with the VELO upgrade design, see Fig. 19.

In practice the impact parameter resolution performance of the VELO is well described by a linear dependence on  $1/p_T$  plus a constant offset. However, the situation is considerably complicated by the presence of the RF foil. The very complex shape gives a significant and highly non uniform contribution to the total material budget. The material traversed before the first measured point has a position and material contribution that varies as a function of pseudorapidity  $\eta$ , azimuthal angle  $\phi$ , and longitudinal position  $z$ . The internal radius is significant, as the closer the foil comes to the interaction region (regardless of the position of the first measured point) the better the impact parameter resolution is expected to be. The amount of material is also significant, and depends on the relative angle of the foil and the track. Although the foil is corrugated in such a way as to present a close to perpendicular face to the particles, there are regions where the tracks pass through significantly greater amounts of material. In the current foil there are also local variations in thickness to be taken into account. Figure 11 shows the detailed material description of the currently installed VELO. The pie chart shows the total amount of

material seen per track, on average, broken down by component. The major contributor is the RF foil, followed by the sensors, and then the hybrids. The plot shows the amount of material before the first measured point, shown as a function of azimuthal and polar angle. The very large local variations in the amount of material are apparent. The comparison with the upgrade design can be seen by referring to Sect. 3.2.

Considerable effort has gone into making the description of the simulation of LHCb, in particular the RF foil, as accurate as possible. The track reconstruction efficiency, impact parameter resolution and primary vertex resolution, extracted using data driven methods, are in good agreement in data and simulation, as shown in Fig. 12. This gives confidence in the simulation as a tool to investigate the expected performance of the upgrade VELO.

## 2.3 Data rate constraints

Imposing a 40 MHz readout results in a huge data rate output needed from the front-end chip, with the number of particle hits per event reaching  $\approx 5.2 \text{ cm}^{-2} \times R^{-1.9}$  at the highest luminosity, where  $R$  is the radius in cm. The mean visible interaction rate is around 27 MHz, however due to variations in the bunch filling scheme the peak rate may reach 40 MHz. In practice, the pixel ASICs must be able to cope with output rates of up to 15.1 Gbit/s and the peak total data rate out of the upgraded VELO can reach 2.85 Tbit/s. Data rates on individual links vary by an order of magnitude. Depending on the amount of buffering that can be achieved in the VeloPix to derandomise the event rate (which follows the beam filling scheme) over the timescale of an orbit, the required output rate may vary from 10.2 (ideal buffering) to 15.1 Gbit/s (no buffering). This translates to link data rates from 2.6 to 3.8 Gbit/s for the most exposed ASICs. These conditions impose some of the most challenging requirements on the VELO upgrade design, in particular the ASIC architecture. For a full discussion see Sect. 6.

## 2.4 Mechanical constraints

The presence of the detector within the LHC beam pipe imposes additional design considerations. In the VELO upgrade design, the concept of separation of primary and secondary vacua is preserved, which imposes requirements on the foil leak tightness, as well as its mechanical stability up to a small pressure difference of 10 mbar. The modules themselves cannot be manufactured out of material which causes excessive outgassing, and great care must be taken with the integrity and leak tightness of the cooling connections. In addition, the overall constraints on the detector geometry, such as the horizontal opening movement, and the total allowed detector length of 1.2 m, remain in place. The requirements are similar to that of the current VELO, however the design considerations have changed considerably, due to the choice of cooling integrated within the module, and the choice of evaporative CO<sub>2</sub> circulating in microchannels. For a more complete discussion see Sect. 9 and 10.

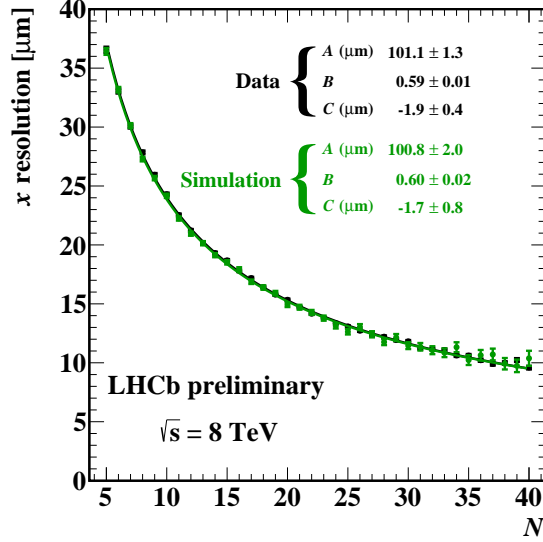
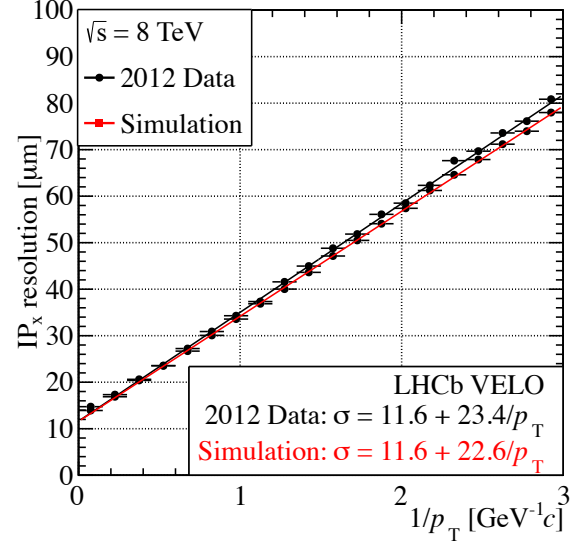
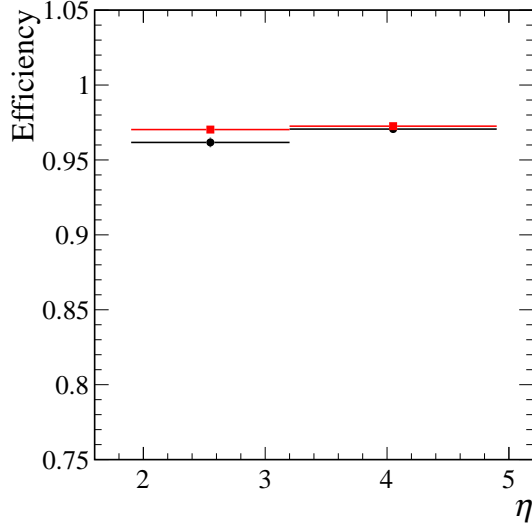


Figure 12: (top left) Tracking efficiency for the current VELO measured in data and simulation using a tag and probe method. (top right) Impact parameter resolution in data and simulation, for the current VELO, shown for the  $x$  component, as a function of the inverse transverse momentum. The resolution is measured relative to the reconstructed primary vertex. (bottom) Primary vertex resolution for the current VELO measured in data and simulation using a data driven method of splitting vertices. For the rest of this document the resolutions and efficiencies are extracted by direct comparison to the simulated tracks and vertices.

## 2.5 Machine interface and VELO aperture

As expressed in Eq. 1, the IP resolution  $\sigma_{\text{IP}}$  is expected to improve (approximately) proportionally to the radius of the first measured point, and it is noteworthy that the multiple scattering term  $\sigma_{\text{MS}}$  is reduced even if the first measured point is kept at a constant radius while the RF foil radius is reduced.

Based on these considerations, and taking into account the experience of several years of stable operation with the current aperture, a series of studies and discussions were carried out with LHC machine experts to identify what minimum radius would be possible for the RF foil [5]. An inner foil radius of 3.5 mm was proposed and agreed upon<sup>2</sup> based on the studies and discussions. This value is still well beyond the limits imposed by machine aperture considerations, while at the same time it leaves enough space for a first sensitive pixel edge at a radius of 5.1 mm, which is about the limit for the pixel chip as determined by the data rate from detailed simulations. The proposed value takes into account the gaps for the guard ring structure (0.5 mm), the foil tolerances (0.5 to 0.8 mm) and the foil thickness (at most 0.3 mm).

Preliminary considerations of the effects of aperture, impedance and dynamic vacuum were performed which show that such an inner radius is acceptable. Wake field simulations with a simplified geometry indicate that the reduction of the inner radius alone was not a show stopper from the point of view of impedance and heat deposition [6]; though careful calculations will be repeated for the final geometry. Dynamic vacuum effects were also simulated for a simplified geometry, from which it can be concluded that the radius reduction is not critical provided that sufficient lateral pumping speed (sideways from the beam axis) as well as a low surface secondary electron yield is maintained [7]. As had been the case for the design of the current VELO, the VELO group is continuing an active cooperation with LHC machine experts to ensure that the final RF shield of the upgrade VELO does not impede safe and reliable operation of the machine.

Although much can be learned and re-used from the current VELO design, the impedance and dynamic vacuum effects will be carefully taken into account while optimizing the final geometry of the upgrade VELO and RF shield. The same principle of electrical continuity will be used as in the current VELO, with the implementation of flexible wake field suppressor elements at the entrance and exit of the VELO vacuum chamber. The depth and pitch of the RF foil corrugations will be kept similar to those of the current VELO RF foil and, for completeness, the impedance effects will be checked by full 3D wake field simulations in cooperation with LHC impedance experts. The foil surfaces exposed directly to beam-induced ion or electron bombardment will be coated with a low activation temperature non-evaporable getter material. Finally, the gaps between the foils will be customized to guarantee sufficient lateral pumping speed and validated with the help of the LHC vacuum group with detailed simulations.

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<sup>2</sup>As a reminder, the current VELO foil inner radius ranges between 4.9 and 5.6 mm, as determined from particle interaction tomography.

## 2.6 Physics performance constraints

The upgraded VELO must provide fast and efficient pattern recognition up to  $\mathcal{L} = 2 \times 10^{33} \text{ cm}^{-2} \text{ s}^{-1}$ . It must have excellent IP resolution and be capable of identifying primary and secondary vertices. The design must be such that fast and efficient selection of events in the event filter farm is possible. These requirements lead to the following design choices:

- Each track in the LHCb acceptance should have a minimum of four spatial measurements.
- The spatial resolution should be the finest possible at the inner radius.
- The minimum radius of the first measured point and the foil position should be the smallest possible.
- There should be minimal material in the fiducial region.

These requirements, together with the experience from the design and operation of the current VELO, and the upgrade requirements imposed by the rest of the LHCb upgrade programme, lead to a set of performance requirements as defined in Table 2.

The numbers as presented in this table represent baseline operation, with no safety margins applied. The module design is expected to satisfy these parameters, while exploring at what stage there is a breakdown in performance, should the limits be exceeded.

The radiation damage is based on simulations, and the required silicon operating temperature is imposed in order to avoid thermal runaway effects, and the maximum tolerable voltage should give signals of 6000 electrons or more at the end of lifetime.

The current cooling system was designed to cool 800 W per side at a temperature of  $-25^\circ\text{C}$ , however in practice the large  $\Delta T$  on the modules led to a lower operational temperature of  $-30^\circ\text{C}$ . In order to guarantee safety at the upgrade it is planned to upgrade the cooling plant to be able to cool 1000 W per side at a lower temperature of between  $-35^\circ\text{C}$  and  $-40^\circ\text{C}$ , and an appropriate safety margin must be built into the module designs. To reach such temperatures the present freon chiller would have to be replaced by a two-stage chiller. A similar cooling plant is presently under construction for the IBL of ATLAS.

The layout parameter constraints reflect the fact that the module ensemble must be compatible with the current vacuum tank and motion system. The module minimum pitch is intended to allow ease of module mounting, as well as room for the additional step of orbital welding the module cooling pipes *in situ*, a step not needed for the current VELO. The module layout is dependent on parameters such as the overall module size; so the requirements are placed on the global module layout rather than the individual module dimensions. Tracks are required to pass from one side to the other for alignment purposes.

Table 2: Overview of VELO upgrade module requirements.

<b>Global parameters</b>	
Radiation tolerance	$8 \times 10^{15} \text{ 1 MeV n}_{\text{eq}}/\text{cm}^2$ at tip
HV tolerance	1000 V
Radiation length	IP resolution as good as current VELO
Outgassing per module	$< 5 \times 10^{-6} \text{ mbar}\cdot\text{l/s}$
Silicon temperature	$< -20^\circ\text{C}$ for $T_{\text{coolant}} = -40^\circ\text{C}$
Operational temperature range	$-40^\circ\text{C}$ to $40^\circ\text{C}$
Max. ASIC power consumption	$3 \text{ W} \times 12 \text{ pixel ASICs}$
Max. total power consumption	$< 1000 \text{ W}$ per side
<b>Module layout parameters</b>	
Max. dimensions per half	$275 \text{ mm (height)} \times 180 \text{ mm (width)}$ $1.2 \text{ m (length)}$
Angular coverage	$2 \leq \eta \leq 5$ at $\sigma_{\text{lumi}} = 63 \text{ mm}$
Number of hits per track	$\geq 4$ for $>99\%$ of tracks
Geometrical efficiency	$> 99\%$ for $R \leq 10 \text{ mm}$
Overlap	Design to include tracks passing from A to C sides
Station pitch	$> 24 \text{ mm}$
<b>General mechanical parameters</b>	
Mechanical deformations	$< 20 \mu\text{m}$ in $x, y$ $< 100 \mu\text{m}$ in $z$
Mounting precision	Tolerance of $< 100 \mu\text{m}$ in $z$ , allow overclosure
Module shape	Impose on foil minimum radius of curvature of $2 \text{ mm}$

### 3 Layout overview

The expected performance of the upgraded VELO was studied using the default LHCb applications for simulation and reconstruction which are also used in the current experiment. For this purpose, the layout of the upgraded VELO was integrated in the LHCb detector description framework and algorithms for simulating the response of sensor and front-end ASIC, clustering of pixel hits, and pattern recognition were developed. A detailed description of the simulation and reconstruction chain can be found in Ref. [8].

#### 3.1 Geometry in simulation

The upgraded VELO consists of two retractable halves, each of which houses an array of 26 L-shaped silicon pixel detector modules (Sect. 3.1.1). The two halves are enclosed in RF boxes which separate the machine vacuum from the secondary vacuum in which the modules are located. The modelling of the thin corrugated walls of the RF boxes facing the beam, the RF foils, is described in Sect. 3.1.2.

##### 3.1.1 Modules

The building blocks of a module are illustrated in Fig. 13 (left). A full description of the module is given in Sect. 5. The description here focusses on the layout as implemented in the simulation.

Each module contains four silicon sensors with a thickness of  $200\text{ }\mu\text{m}$  and an active area of  $42.46 \times 14.08\text{ mm}^2$ , surrounded by an inactive edge with a width of  $450\text{ }\mu\text{m}$ .

A sensor is bump-bonded to a row of three VeloPix ASICs. The ASICs, which feature an active area of  $14.08 \times 14.08\text{ mm}^2$ , are modelled as  $200\text{ }\mu\text{m}$  thick blocks of silicon.

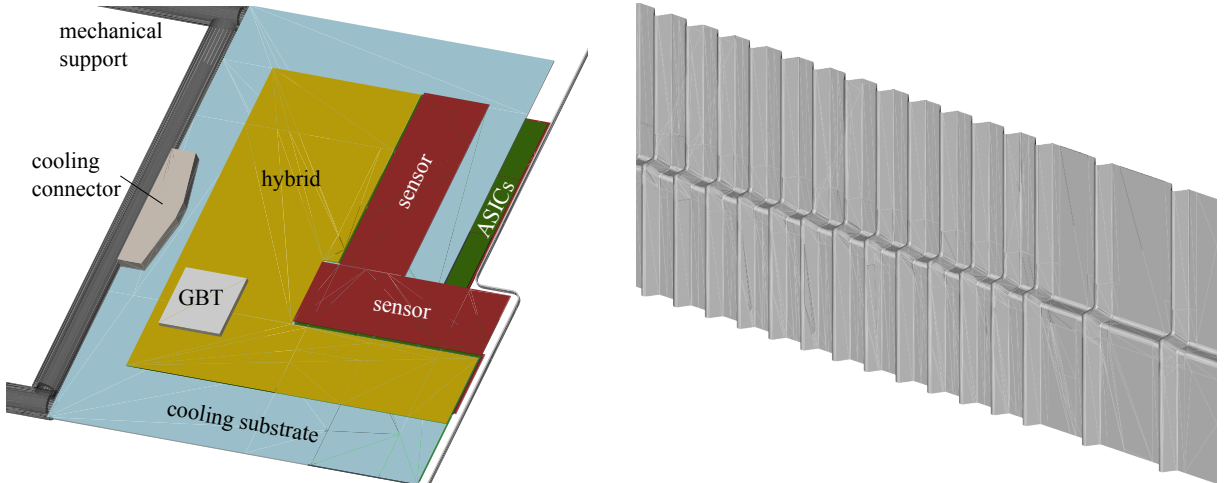


Figure 13: (left) Layout of a module, as implemented in the LHCb simulation framework, showing the positions of the major components, including a cross section of the RF foil at the  $z$ -position of the module. (right) A view of the upgraded RF foil.

Table 3: System parameters of the VELO upgrade.

# modules	52
# ASICs per module	12
# ASICs total	624
# silicon sensors	208
silicon sensor thickness	200 $\mu\text{m}$
# pixels	41 M
pixel dimensions	$55 \times 55 \mu\text{m}^2$
position of first station upstream	-289 mm
position of last station downstream	751 mm
radiation level at 5.1 mm radius	$1.1 - 1.8 \times 10^{14} \text{1 MeV n}_{\text{eq}}/\text{fb}^{-1}$
radiation level at 50 mm radius	$1.7 - 2.6 \times 10^{12} \text{1 MeV n}_{\text{eq}}/\text{fb}^{-1}$
Total active area	1243 $\text{cm}^2$
Peak total data rate	2.85 Tbit/s
# optical links	1664

The two assemblies of sensor and ASICs (tiles) which are aligned vertically are mounted on opposite sides of the module, as are the two horizontal tiles. In order to ensure full coverage for angled tracks, the active areas of front and back side assemblies overlap by  $110 \mu\text{m}$ . As the inner horizontal tile is located on the same side as the outer vertical tile, the latter needs to be displaced by 1 mm with respect to the inner vertical tile, resulting in a small acceptance gap. The inner tiles of left and right module form a square acceptance “hole”, with the boundaries of the pixel cells closest to the beam being located at  $x, y = \pm 5.1 \text{ mm}$ .

The microchannel cooling substrate is represented by a  $400 \mu\text{m}$  thick silicon slab. In order to minimise the material budget before the first measured point on a track, the substrate is retracted by 5 mm with respect to the inner boundary of the active area. The 2.5 mm thick cooling connector and its 1 mm thick counter-piece, both made of stainless steel, are mounted at the edge of the substrate ( $x = \pm 80 \text{ mm}$ ).

For the remaining module components, simplified descriptions are used. The hybrids are approximated by a  $450 \mu\text{m}$  thick layer of kapton and a  $30 \mu\text{m}$  thick layer of copper, and the GBTx chip is modelled as a 1 mm thick silicon block with the same lateral dimensions as the VeloPix. The modules are held in place by carbon-fibre bars with an outer diameter of 6 mm and a wall thickness of 1 mm. It is anticipated that the description will be refined and missing components such as readout cables and cooling pipes will be added once the detailed design is finalised.

A summary of some basic parameters of the upgrade VELO is presented in Table 3.



### 3.1.2 RF foil

Experience from the existing VELO has shown that an accurate description of the RF foil in the simulation is a crucial ingredient to describe the spatial resolution of tracks and vertices. The complex shape of the upgraded RF foil is described by a mesh of trapezoidal elements. As can be seen from Fig. 13 (right), the foil follows the L-shape of the modules. At the module positions the closest horizontal and vertical distance of the foil to the beamline is 3.5 mm. In the flat sections between the module slots the foil is further away from the beam, with a closest distance of 10 mm. In the central region, the length of the flat sections is 9 mm. As in the existing VELO, the RF foil is made of aluminium, but has a uniform thickness of 250  $\mu\text{m}$  (compared to the existing foil which has a nominal thickness of 300  $\mu\text{m}$  and exhibits local thickness variations).

### 3.1.3 $z$ layout

The  $z$ -layout was designed so that 99% of tracks within the nominal LHCb acceptance which originate from within  $\pm 2\sigma_{\text{lumi}}$  of the interaction point cross at least four stations in the VELO. The spacing between central stations is thus given by

$$\Delta z = \frac{R_{\text{out}} - R_{\text{in}}}{4 \tan(\theta_{\text{max}})} ,$$

where  $\theta_{\text{max}} = 269 \text{ mrad}$ , corresponding to  $\eta = 2$ , is the largest polar angle to be within the acceptance,  $R_{\text{in}}$  is the inner radius and  $R_{\text{out}}$  the outer radius of the sensitive area of a VELO module.

For the square pixel module, different sets of radii can be considered. Tracks parallel to the  $x$  or  $y$  axis (on-axis tracks,  $\phi = 0, 90, 180, 270^\circ$ ) are more important when calculating the spacing between the central stations. For these tracks the radii are  $R_{\text{in}} = 5.1 \text{ mm}$  and  $R_{\text{out}} = 33.15 \text{ mm}$ , which gives  $\Delta z = 25 \text{ mm}$ .

Next the downstream stations are considered, these stations start at a  $z$ -position such that they can measure tracks with the smallest angle within the LHCb upgrade acceptance  $\theta_{\text{min}}$  ( $\eta = 5$ ). The  $z$ -position is determined using

$$z = \frac{R_{\text{in}}}{\tan \theta_{\text{min}}} + 2\sigma_{\text{lumi}}$$

and assuming that  $\sigma_{\text{lumi}} = 63 \text{ mm}$ . In this case tracks at a 45, 135, 225, 315° angle to the  $x$ -axis (off-axis tracks) are more important than on-axis tracks and so  $R_{\text{in}} = 7.2 \text{ mm}$  is used to calculate the start of this region to be  $z = 660 \text{ mm}$ .

A ray tracing simulation is used to determine a set of module positions which satisfies the 99% efficiency requirement. A 24-station layout is chosen, with the central stations spaced 25 mm apart and spanning the region from  $z = -68 \text{ mm}$  to  $z = 257 \text{ mm}$ , and with the first downstream station positioned at  $z = 610 \text{ mm}$ .

Ideally the central region would continue further upstream, but since only 52 modules can be cooled by the cooling plant, several stations are omitted; this means backwards

tracks with low  $|\eta|$  are not always detected. To measure high  $|\eta|$  backwards tracks the upstream modules would need to be much further away, however the size of the RF box limits the position of the modules in this direction. The ray tracing simulation was used to roughly optimise the five upstream stations to have the highest number of backwards tracks with four hits, which resulted in the current layout. Further full LHCb simulation studies will be needed to optimise the upstream stations.

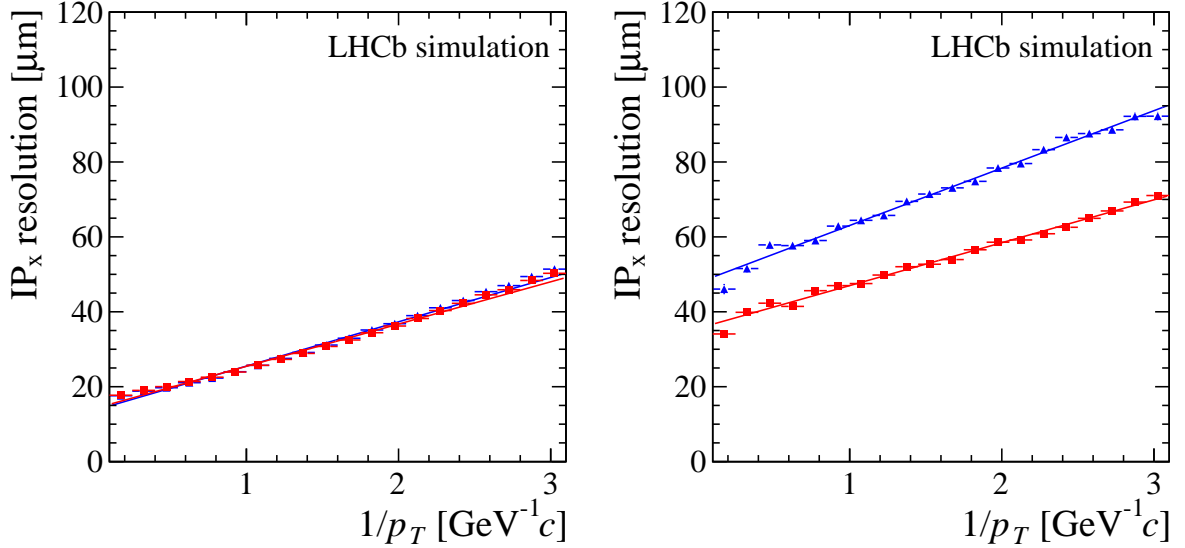


Figure 14: IP resolution in the  $x$ -direction (blue triangles) for a layout optimised by ray-tracing and (red circles) for the layout optimised using the full simulation. This is shown (left) for tracks with first hit  $z < 300$  mm and (right) tracks with first hit  $z > 300$  mm.

The full LHCb simulation is used to optimise the downstream stations, specifically the spacing between the last four stations and also the number stations in the region  $300 \text{ mm} < z < 600 \text{ mm}$ . This optimisation minimised the IP resolution while maintaining the acceptance. In the layout from the ray-tracing optimisation, the IP resolution of tracks with the first hit at  $z > 300$  mm is substantially worse compared to those with a hit in the central region. The IP resolution of tracks generally can be improved in two ways, by reducing the extrapolation distance from the first hit to the primary vertex or by having a larger distance between hits to give a larger lever arm. The first is done by adding two further stations in the region  $300 \text{ mm} < z < 600 \text{ mm}$ . This gives approximately a 20% improvement in IP resolution for tracks with a first hit at  $z > 300$  mm. Increasing the spacing between the last four stations to 45 mm further improves the IP resolution of these tracks by 20%. Despite adding two extra stations downstream of the interaction point, there is little change in the IP resolution of tracks with a first hit in the central stations, as shown in Fig. 14. Considering all tracks the IP resolution is improved by  $\sim 7\%$  compared to the layout optimised using only ray-tracing. This optimised layout for the upgraded VELO is compared to the current VELO layout in Fig. 15 and the exact module positions

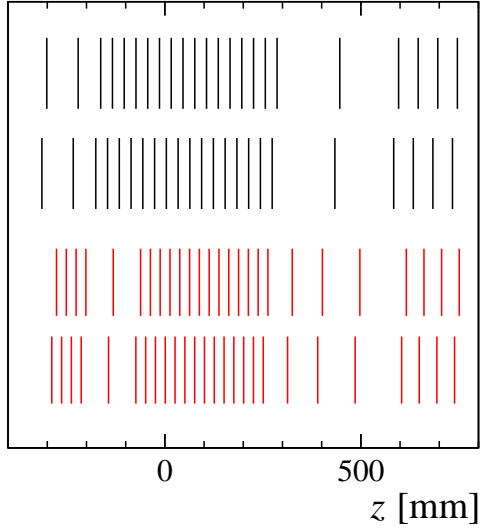


Figure 15: Comparison of current and upgrade VELO  $z$ -layouts. Top layout (black): current VELO. Bottom layout (red): upgrade VELO optimised with full-simulation.

Table 4: Optimised  $z$ -positions of the 52 modules of the VELO upgrade, split by side. A side is also known as the left side and is in the positive  $x$ -direction. C side is also known as the right side and is in the negative  $x$ -direction. The  $z$ -positions are given in mm from the interaction point.

Side	Module $z$ -position [mm]								
A	-277.0	-252.0	-227.0	-202.0	-132.0	-62.0	-37.0	-12.0	13.0
	38.0	63.0	88.0	113.0	138.0	163.0	188.0	213.0	238.0
	263.0	325.0	402.0	497.0	616.0	661.0	706.0	751.0	
C	-289.0	-264.0	-239.0	-214.0	-144.0	-74.0	-49.0	-24.0	1.0
	26.0	51.0	76.0	101.0	126.0	151.0	176.0	201.0	226.0
	251.0	313.0	390.0	485.0	604.0	649.0	694.0	739.0	

for the upgraded VELO are listed in Table 4. The acceptance of the optimised layout is shown in Fig. 16 from the ray-tracing simulation.

### 3.2 Material scan

The material budget of the upgraded VELO is evaluated by following straight-line tracks from the origin to the plane  $z = 835$  mm. For each volume traversed by the track, the radiation length of the material and the length of the track segment inside the volume are recorded. Figure 17 shows the resulting integrated fraction of the radiation length  $x/X_0$  as function of  $\phi$  and  $\eta$ . The most prominent features in the material map are the ridges due to the RF foil at  $\phi = \pm\pi/2$  and the peaks due to the cooling connector at  $\phi = 0, \pi$ . Averaged over the nominal pseudorapidity range  $2 < \eta < 5$ , the total material

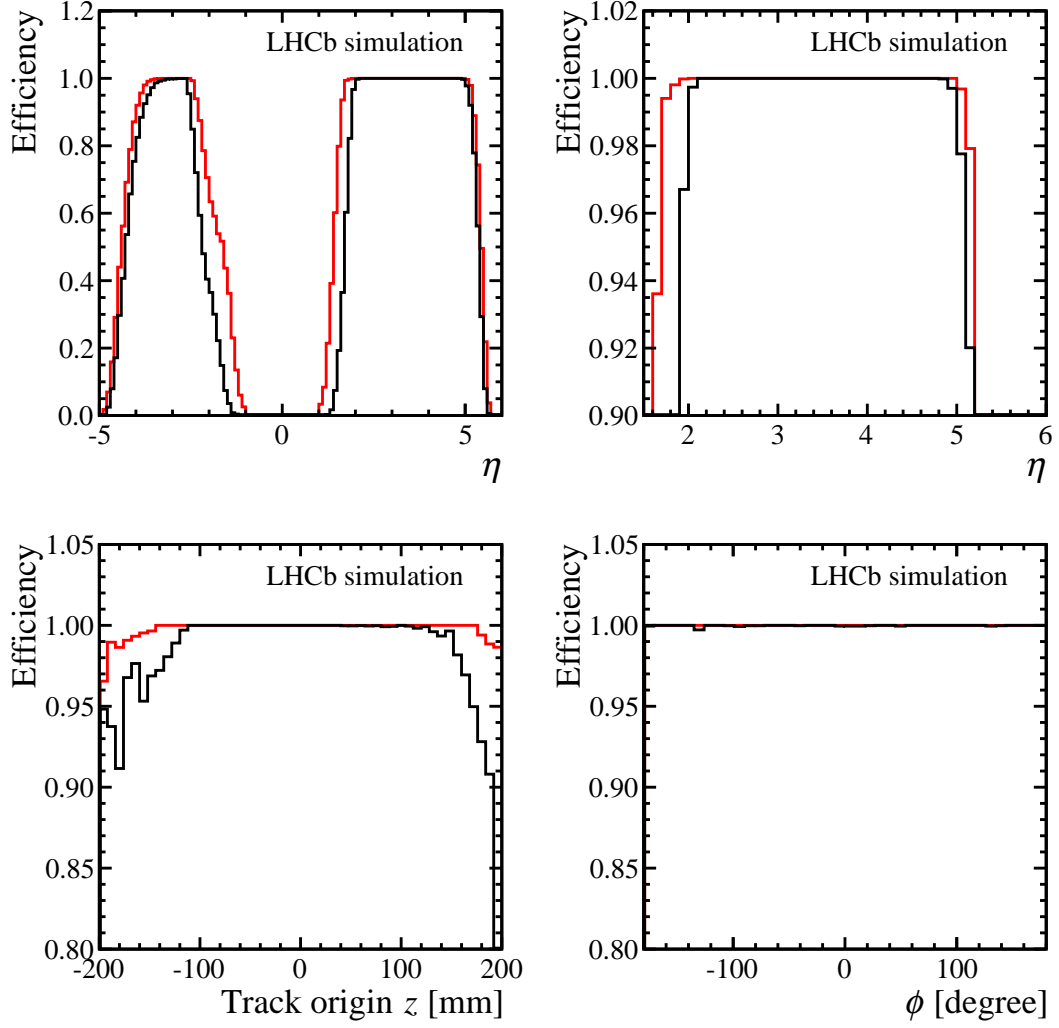


Figure 16: Fraction of tracks with (red) three or (black) four hits from ray-tracing simulation as a function of different variables. Top row: different regions of  $\eta$ , requiring the track came from  $\pm 2\sigma_{\text{lumi}}$  of the interaction region. Bottom left: track origin  $z$ -position, requiring  $2 < \eta < 5$ . Bottom right:  $\phi$ , requiring the track came from  $\pm 2\sigma_{\text{lumi}}$  of the interaction region and was between  $2 < \eta < 5$ .

budget of the upgraded VELO amounts to  $\sim 21.3\% X_0$ , which is similar to the existing VELO (20.0%). As can be seen from Fig. 19 (left), the largest contribution ( $\sim 53\%$ ) comes from the RF foil. This is also visible in Fig. 18 which shows the material map projected onto the  $\eta$  and  $\phi$  axes. Figure 18 also shows the contributions from material before the first and second measured points, respectively. These are important quantities for the IP distribution and the extrapolation of VELO tracks to the downstream tracking. Averaged over  $2 < \eta < 5$ , the material before the first measured point amounts to  $\sim 1.7\% X_0$ . As

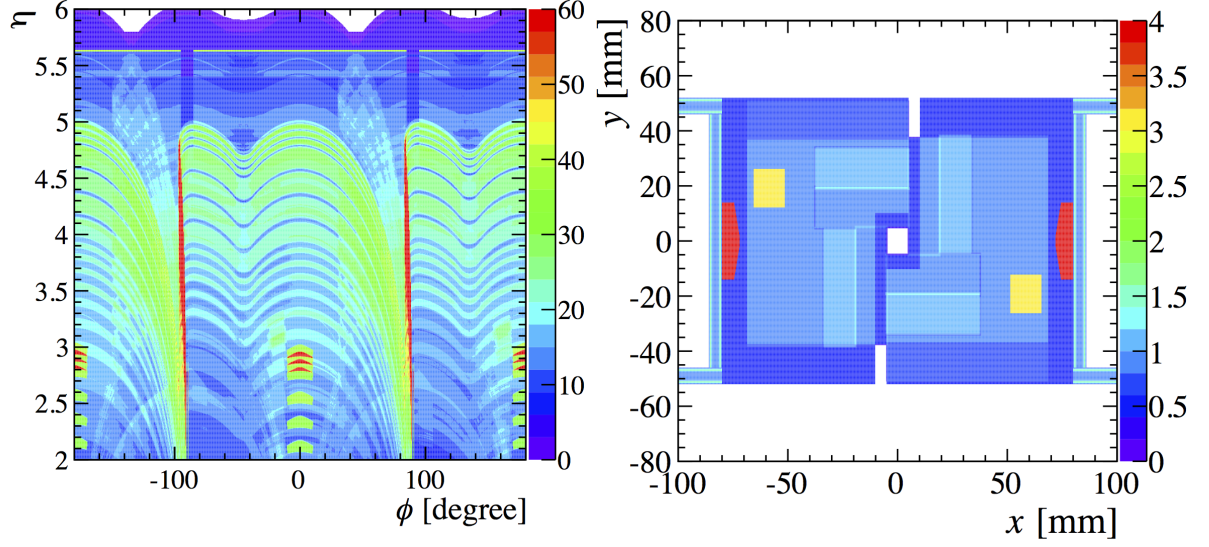


Figure 17: Percentage of a radiation length (between the origin and  $z = 835$  mm) seen by tracks traversing the upgrade VELO (left) as function of  $\eta$  and  $\phi$  and (right) percentage of a radiation length seen by tracks crossing a VELO station (excluding the RF foil) at perpendicular incidence. Averaged over  $2 < \eta < 5$ , the total material budget of the upgrade VELO is  $\sim 21.3\% X_0$ . Averaged over the area  $|x| < 33$  mm,  $|y| < 33$  mm (excluding the inner acceptance “hole”), the material budget of a module is  $\sim 0.94\% X_0$  (for perpendicularly incident tracks).

can be seen by comparing Figs. 19 (right) and 11 (right), this is a significant reduction (by a factor 2.7) with respect to the existing VELO.

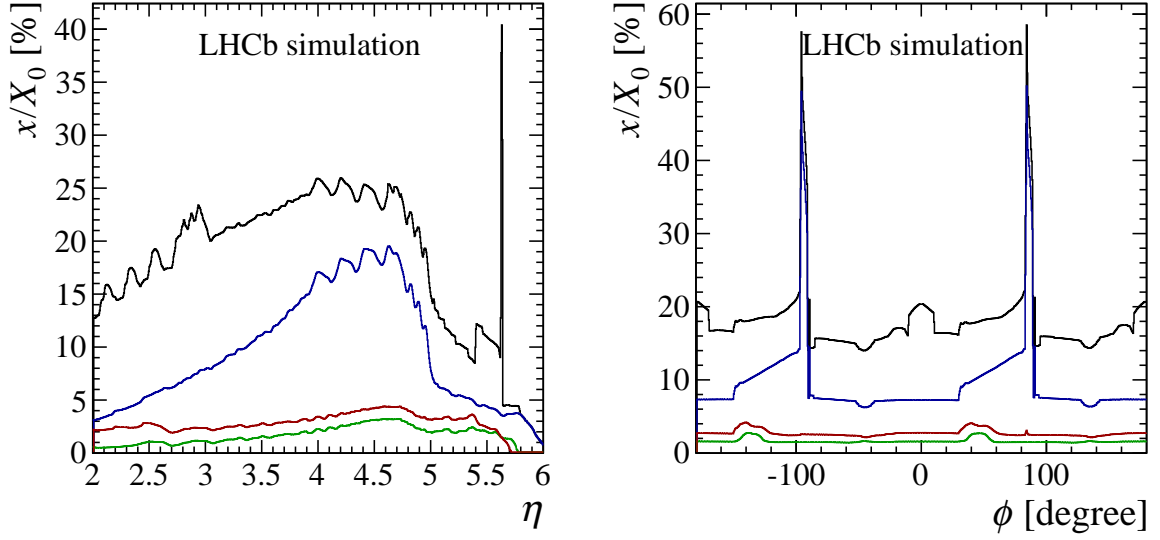


Figure 18:  $x/X_0$  as function of pseudorapidity averaged over  $\phi$  (left) and as function of azimuth averaged over  $2 < \eta < 6$  (right). The black curves show the total material budget, the blue curves the contribution from the RF foil, the red curves the contribution from material before the second measured point, and the green curves the contribution from material before the first measured point.

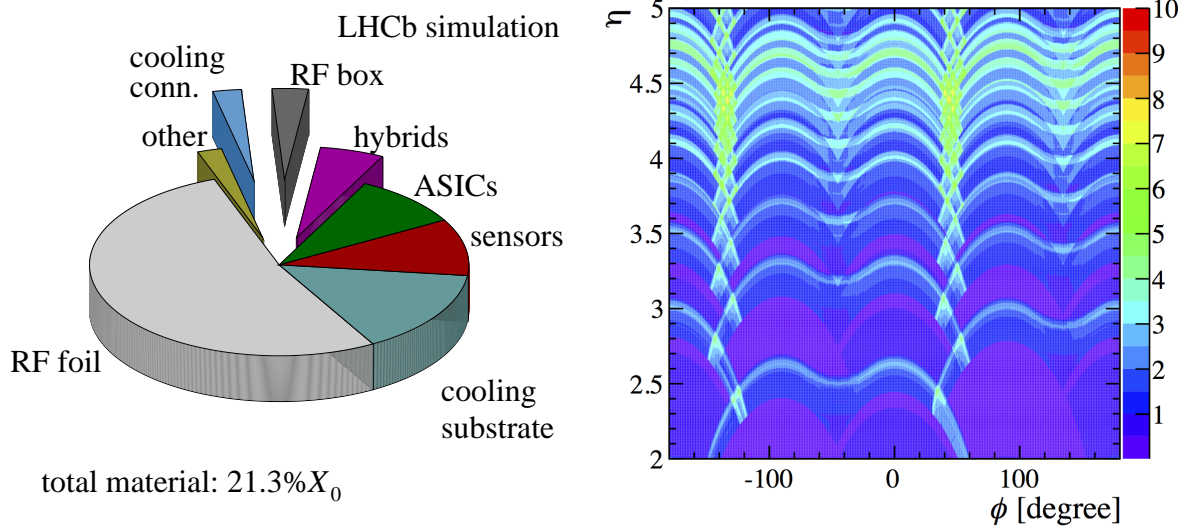


Figure 19: (left) Pie chart showing the contributions from different components to the total material budget in the upgraded VELO within the pseudorapidity range  $2 < \eta < 5$ . (right) Percentage of the radiation length before the first measured point as function of pseudorapidity and azimuthal angle (average:  $x/X_0 \sim 1.7\%$ ).

## 4 Performance

This section covers the performance evaluation of the upgraded VELO. Key measures of the performance including the hit resolution, track reconstruction efficiency and decay time resolution were studied in detail using the simulation and reconstruction software discussed in Sect. 3.

Unless stated otherwise, the figures of merit – both for the current and the upgrade VELO – were produced using samples of simulated minimum-bias events at an average number of interactions per bunch crossing of  $\nu = 7.6$  corresponding to an instantaneous luminosity of  $2 \times 10^{33} \text{ cm}^{-2} \text{ s}^{-1}$  (see Table 1).

### 4.1 Occupancy

The occupancy decreases as a function of radius as the pixel pitch is constant over the whole detector. It is highest for the station closest to the interaction point. As can be seen from Fig. 20, the pixels in this station which are closest to the beamline exhibit an occupancy of  $\sim 0.125\%$ . The difference between cluster occupancy and pixel occupancy reflects the average cluster size ( $\sim 2$  at a threshold of 1000 electrons). The average number of particles crossing a VeloPix ASIC in one minimum-bias event varies between 8.5 for the “hottest” ASIC and  $< 1$  for the outermost ASIC.

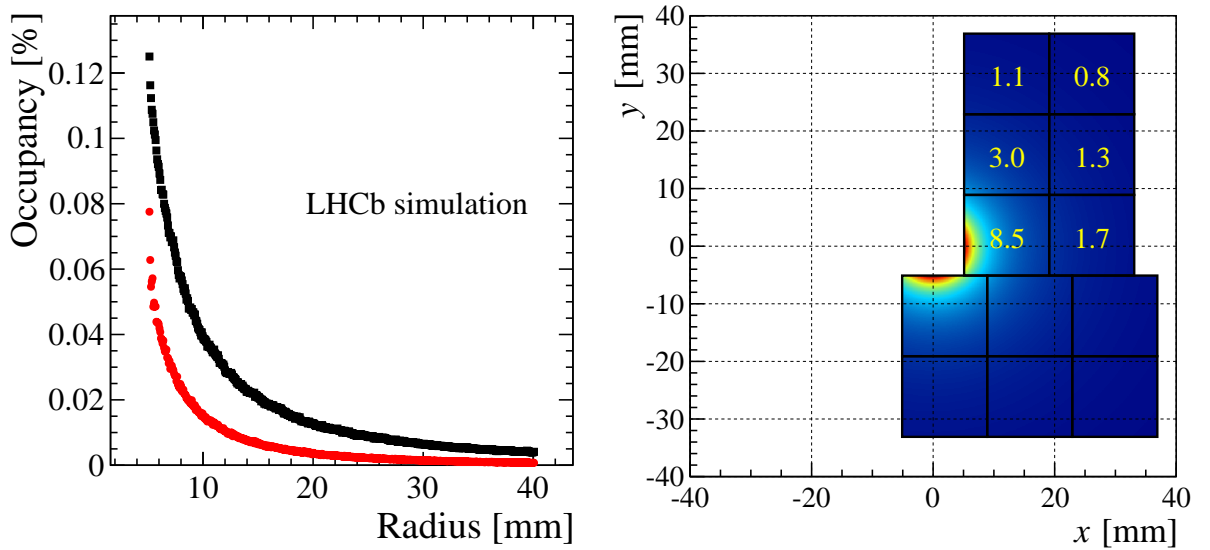


Figure 20: (left) Pixel occupancy (black squares) and cluster occupancy (red circles) as function of radius for the station closest to the nominal interaction point. (right) Mean number of particles crossing an ASIC per event. In the background, the particle density is shown on an arbitrary linear scale.

## 4.2 Hit resolution

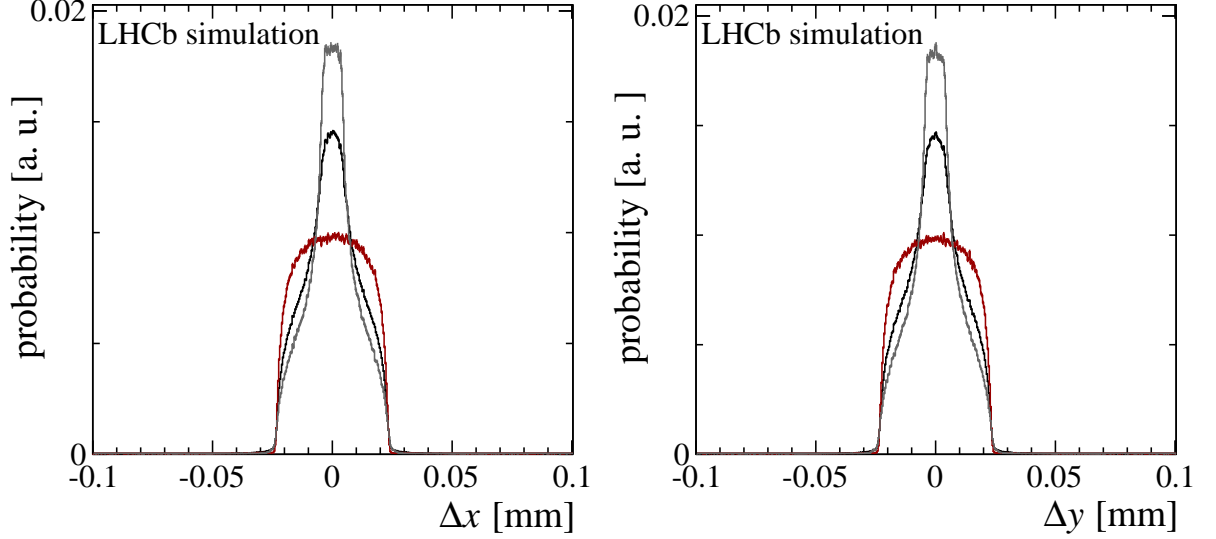


Figure 21: Residual distribution of (left) global  $x$ -coordinates and (right) global  $y$ -coordinates for (red) single-pixel clusters, (grey) two-pixel clusters and (black) all clusters.

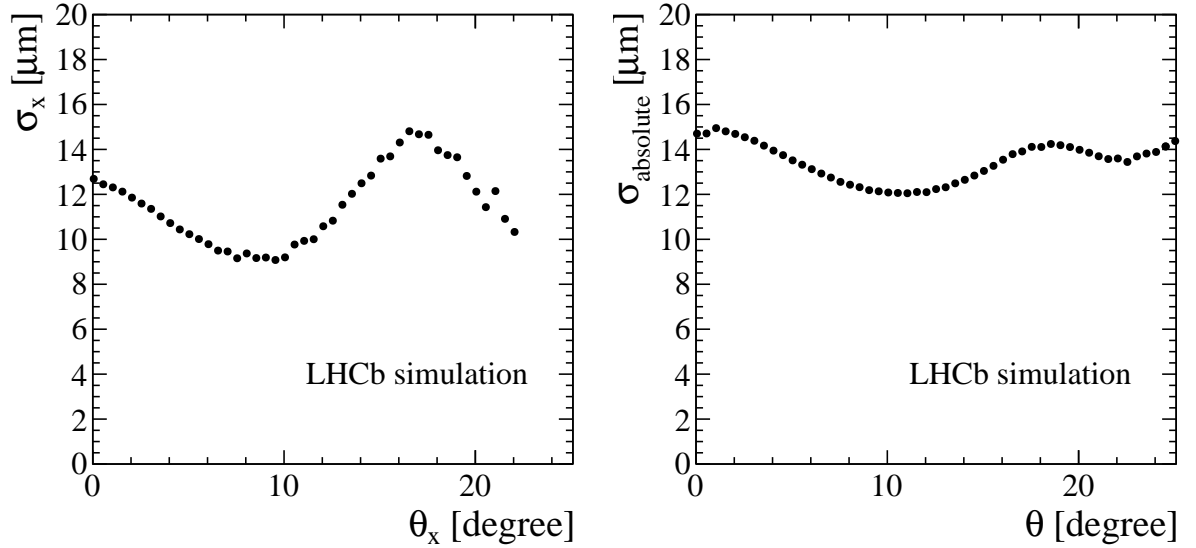


Figure 22: (left) Resolution in the  $x$  direction for small angles  $\theta_y$ . (right) Absolute measurement error versus track polar angle.

In the binary readout scheme the position of a cluster is calculated as the simple average of the individual pixel positions. Figure 21 shows the distributions of the differences



between the global  $x, y$  coordinates of the reconstructed cluster and the coordinates of the associated simulated hit. The distributions are shown separately for single-pixel clusters (which constitute  $\sim 45\%$  of all clusters) and two-pixel clusters (which constitute  $\sim 37\%$  of all clusters). Averaged over all cluster sizes, the RMS of the residual distribution is approximately  $12\text{ }\mu\text{m}$  in both  $x$  and  $y$ .

In addition to the cluster size, the residual distribution also depends on the angle  $\theta$  between the track and the normal vector of the sensor plane. Figure 22 (left) presents the single hit resolution in  $x$ , defined as the RMS of the residual distribution, versus the projected angle  $\theta_x$ , for tracks with  $|\theta_y| < 2^\circ$ . It can be seen that there is an optimal resolution for tracks with angles close to  $9^\circ$ . Figure 22 (right) shows the absolute measurement error, defined as the average absolute distance between the true and reconstructed position, as a function of  $\theta$ , integrated over all azimuthal angles.

### 4.3 Track reconstruction

The pattern recognition for the upgraded VELO starts by looking for pairs of unused hits on neighbouring stations which are compatible with track slopes  $|dx/dz| < 0.4$ ,  $|dy/dz| < 0.4$ . These seed tracks are then extrapolated in the upstream direction and the closest hit within a search window around the predicted position on a sensor is added if it passes a cut on the maximal scattering angle. In case of tracks comprising only three hits, all hits are required to be unused by other track candidates.

#### 4.3.1 Reconstruction efficiency

The efficiency of the pattern recognition algorithm is measured in simulation by comparing the number of correctly reconstructed tracks to the number of reconstructible tracks obtained from truth information. In the LHCb tracking framework the following definitions are used:

- A particle is reconstructible as a VELO track if there are clusters associated to it on three or more modules. In case of the current VELO, hits in three  $R$  and three  $\phi$  sensors are required.
- A particle is reconstructible as a “long track” if it is reconstructible as a VELO track and, in addition, has at least one  $x$  and one “stereo” hit in each of the three downstream track seeding stations.
- A particle is considered reconstructed if at least 70% of the measurements on a track are associated to this particle.
- A ghost track or fake track is a track which cannot be associated to any simulated particle. If more than one reconstructed track is associated to a particle the extra tracks are counted as clone tracks.

Table 5: Pattern recognition performance parameters for current and upgrade VELO at upgrade beam conditions ( $\nu = 7.6$ ,  $\sqrt{s} = 14$  TeV) and for the current VELO at 2011 beam conditions ( $\nu = 2$ ,  $\sqrt{s} = 7$  TeV). For the reconstruction efficiency, the following categories are considered: all particles reconstructible in the VELO with  $p > 5$  GeV/ $c$ , all particles reconstructible as long tracks with and without a momentum cut of 5 GeV/ $c$ , and particles from decays of  $b$ -hadrons with and without a momentum cut of 5 GeV/ $c$ . These parameters were measured using simulated events containing the decay  $B^0 \rightarrow K^{*0} \mu^+ \mu^-$ .

	Existing VELO [%]		Upgraded VELO [%]
	$\nu = 2$	$\nu = 7.6$	$\nu = 7.6$
Ghost rate	6.2	25.0	2.5
Clone rate	0.7	0.9	1.0
Reconstruction efficiency			
VELO, $p > 5$ GeV/ $c$	95.0	92.7	98.9
long	97.9	93.7	99.4
long, $p > 5$ GeV/ $c$	98.6	95.7	99.6
$b$ -hadron daughters	99.0	95.4	99.6
$b$ -hadron daughters, $p > 5$ GeV/ $c$	99.1	96.6	99.8

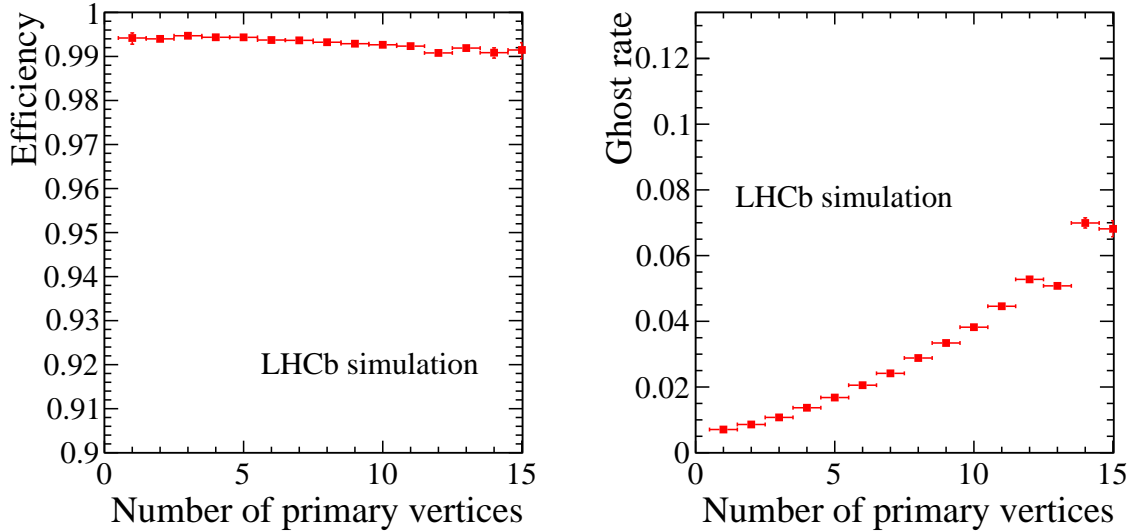


Figure 23: Pattern recognition performance of the upgrade VELO as function of the number of primary vertices, measured using simulated events containing the decay  $B^0 \rightarrow K^{*0} \mu^+ \mu^-$  (left: reconstruction efficiency for particles reconstructible as long tracks, right: ghost rate).

The pattern recognition efficiency,

$$\varepsilon_{\text{rec}} = \frac{N_{\text{reconstructed and reconstructible}}}{N_{\text{reconstructible}}}, \quad (2)$$

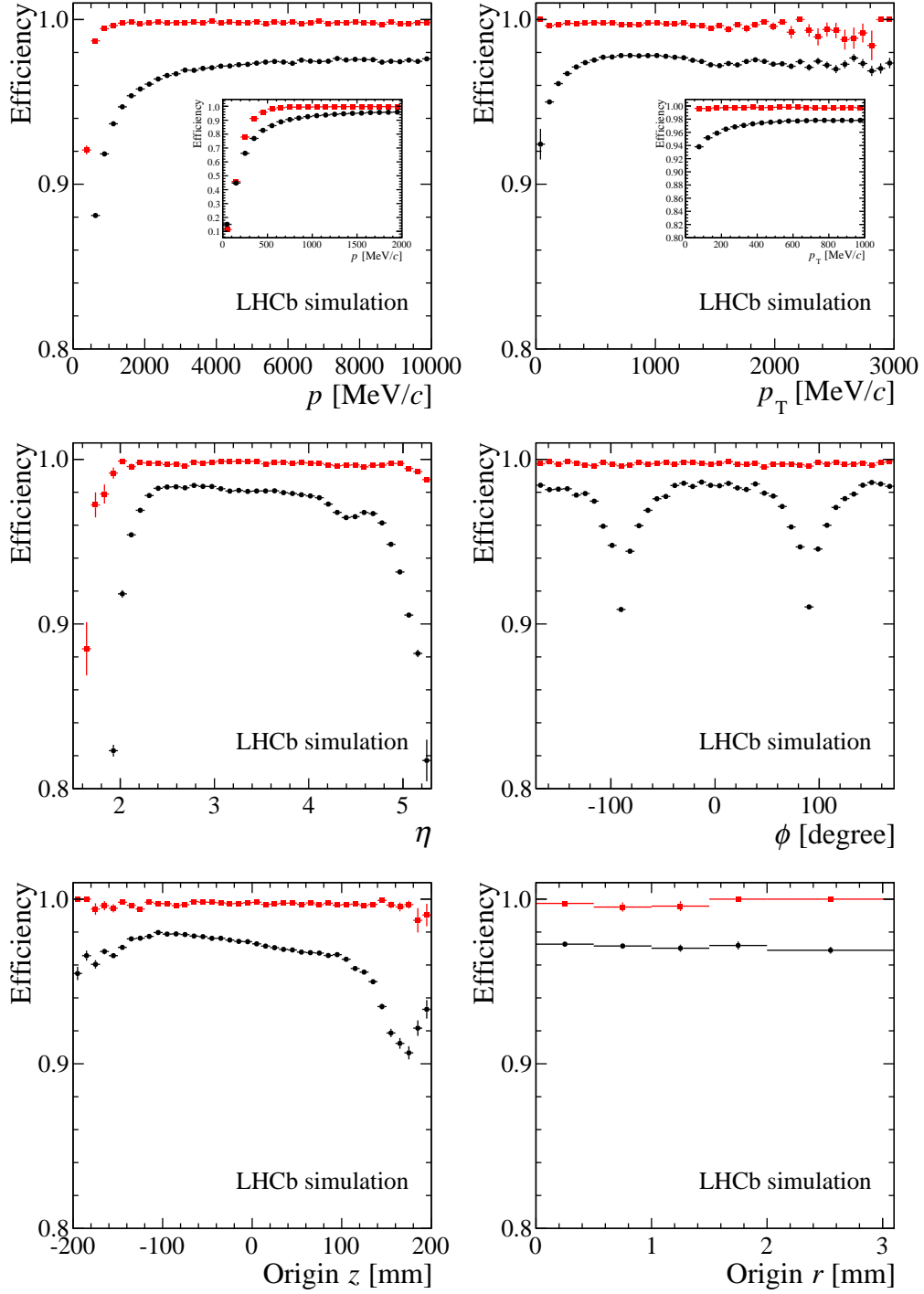


Figure 24: Reconstruction efficiency (at  $\nu = 7.6$ ,  $\sqrt{s} = 14$  TeV) for particles which are reconstructible as VELO tracks as a function of (top left) particle momentum, (top right) transverse momentum, (middle left) pseudorapidity, (middle right) azimuthal angle, (bottom left) origin vertex  $z$ -position and (bottom right) origin vertex radius. The requirements a track has to satisfy to be reconstructible are listed in the text. The current VELO is shown with black circles and the upgrade VELO with red squares. The insets show the low momentum and transverse momentum regions.

for the upgrade and the current VELO at an instantaneous luminosity of  $2 \times 10^{33} \text{ cm}^{-2} \text{ s}^{-1}$  is detailed in Table 5, together with the reconstruction efficiency of the existing VELO at 2011 beam conditions. It can be seen that the efficiency of the upgraded VELO at upgrade beam conditions is superior to that of the existing VELO, both at upgrade and 2011 beam conditions. Table 5 also shows that the ghost rate in the upgraded VELO is significantly lower. It should be noted however, that the pattern recognition algorithm for the current VELO was not optimised for the occupancy level anticipated in the LHCb upgrade.

It is also interesting to investigate the performance as a function of the number of primary vertices. This gives an indication of the robustness against increases in pile-up. Fig. 23 shows the behaviour of the tracking efficiency and ghost rate; two parameters which are expected to be most sensitive to this quantity. It can be seen that from an algorithmic point of view the performance of the upgrade VELO is very robust against increases in pile-up. These plots do not take into account hardware limitations, notably that as the occupancy of the hottest pixels increases there will be a gradual increase in inefficiency (see Sect. 6.4), however initial studies indicate that the effect on VELO performance will be very small. The global data output capabilities of the upgrade VELO are discussed more extensively in Sects. 6 and 7.

In Fig. 24 the pattern recognition efficiency for particles reconstructible as VELO tracks is shown as a function of various track variables: momentum  $p$ , transverse momentum  $p_T$ , pseudorapidity  $\eta$ , azimuthal angle  $\phi$ ,  $z$ -position and origin vertex radius. The performance for both the current and the upgrade VELO are evaluated at upgrade beam conditions ( $\nu = 7.6$ ,  $\sqrt{s} = 14 \text{ TeV}$ ). In these figures, the following additional requirements were made for both the numerator and the denominator (except in those plots where the quantity concerned itself is displayed).

- The pseudorapidity must lie in the range  $2 < \eta < 5$ .
- The track must have  $p > 5 \text{ GeV}/c$ .
- The radius of the origin vertex must be less than 1 mm.
- The  $z$ -position of the origin vertex must be within  $\pm 2\sigma_{\text{lumi}} = \pm 126 \text{ mm}$ .

The upgrade VELO shows high efficiency over virtually the whole range of the variables considered.

#### 4.3.2 Hit efficiency

The average number of hits per track as a function of  $\phi$ ,  $\eta$  and the track origin vertex  $z$ -position is shown in Fig. 25, for tracks which satisfy the requirements on momentum,  $\eta$  and origin vertex position listed in Sect. 4.3.1. The upgrade VELO has more hits per track than the current VELO in order to guarantee four hits per track for all azimuthal angles. For instance in the central region the spacing between modules could be as large as 36 mm for off-axis low- $\eta$  tracks, but for on-axis low- $\eta$  tracks it needs to be 25 mm (see

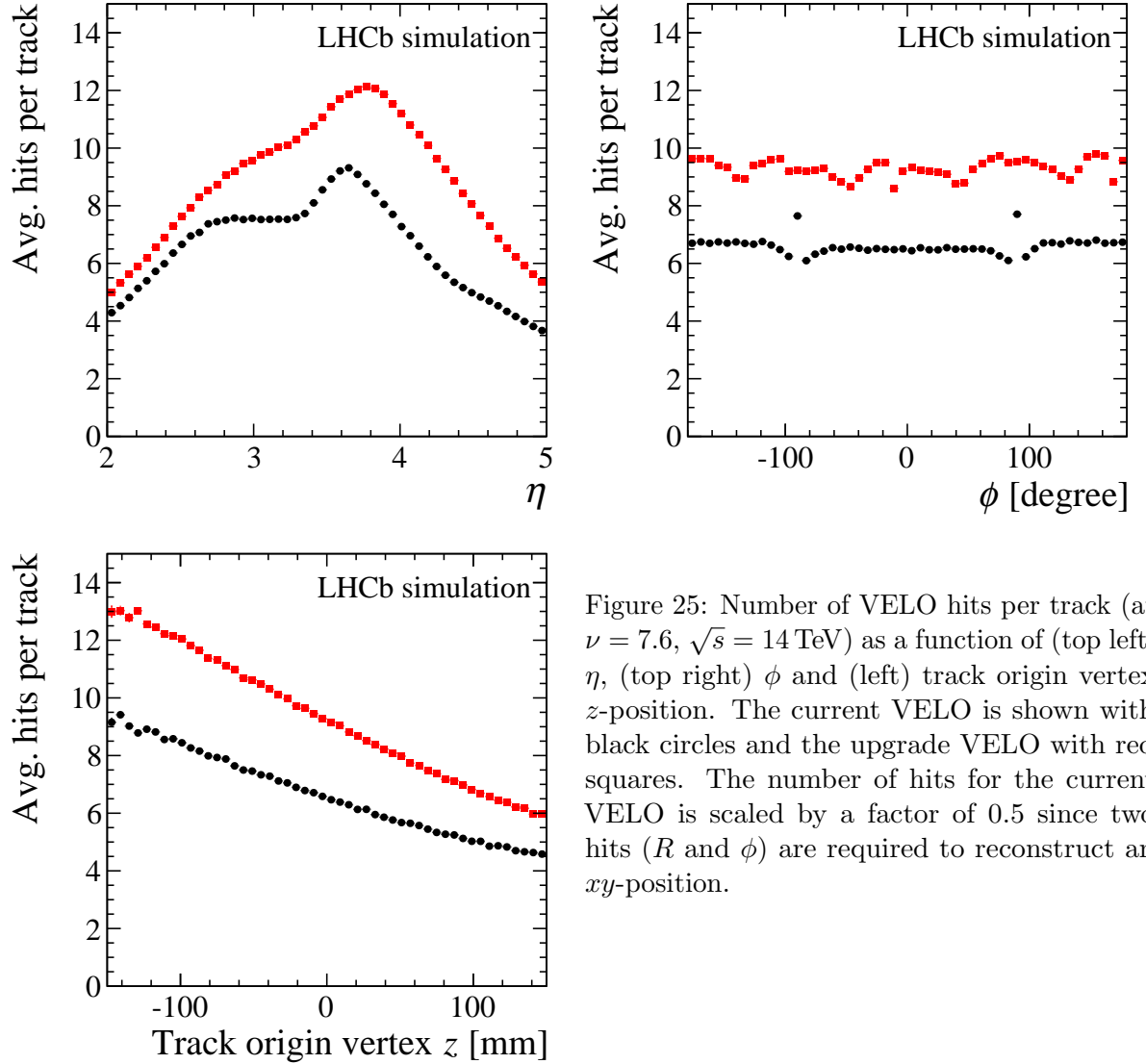


Figure 25: Number of VELO hits per track (at  $\nu = 7.6$ ,  $\sqrt{s} = 14$  TeV) as a function of (top left)  $\eta$ , (top right)  $\phi$  and (left) track origin vertex  $z$ -position. The current VELO is shown with black circles and the upgrade VELO with red squares. The number of hits for the current VELO is scaled by a factor of 0.5 since two hits ( $R$  and  $\phi$ ) are required to reconstruct an  $xy$ -position.

Sect. 3.1.3). This means that for  $\eta = 2$  tracks there are on average more than four hits per track. For  $\eta = 5$  tracks the additional hits are needed to improve the IP resolution.

The hit efficiency is shown in Fig. 26 as a function of  $\phi$ ,  $\eta$  and the origin vertex  $z$ -position. This is defined as the number of hits on a reconstructed track which are associated to a simulated particle divided by the number of hits the simulated particle should have produced. On average the upgrade VELO has a higher hit efficiency than the current VELO. The inefficiency in the upgrade VELO is mostly caused by the tracking algorithm; by design the algorithm does not look for a second hit on the same module, which does occasionally happen.

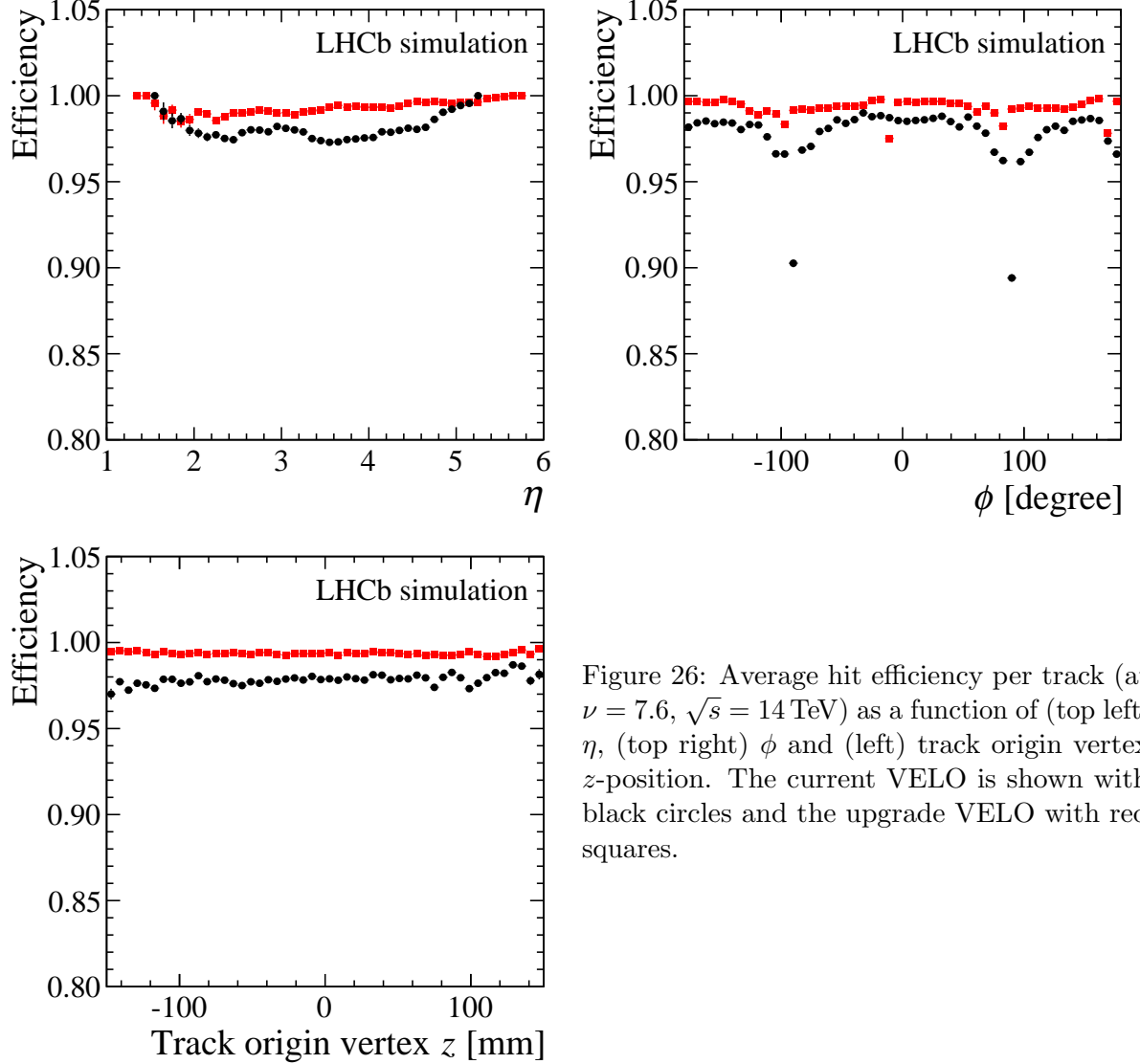


Figure 26: Average hit efficiency per track (at  $\nu = 7.6$ ,  $\sqrt{s} = 14$  TeV) as a function of (top left)  $\eta$ , (top right)  $\phi$  and (left) track origin vertex  $z$ -position. The current VELO is shown with black circles and the upgrade VELO with red squares.

#### 4.3.3 Timing

The trigger strategy for the upgraded LHCb detector is based on accessibility of the full event information at each level of the trigger, including whether tracks originate from displaced vertices that are characteristic of heavy flavour decays. In order to supply displaced vertex information at the earliest stages of the trigger, a tracking system with rapid pattern recognition is essential. For the upgrade the whole detector will be read out at 40 MHz and each event analysed in a trigger system implemented in software. A detector upgraded in this way would allow the yield of hadronic  $B$  decays to be increased by an order of magnitude for the same LHC machine run-time [2].

The first step of the software trigger is to reconstruct all track segments in the VELO using the full pattern recognition. The CPU time consumed by the trigger algorithms is

one of the most crucial parameters of the trigger system.

The performance was evaluated on a sample of simulated minimum bias events generated with beam conditions corresponding to an instantaneous luminosity of  $2 \times 10^{33} \text{ cm}^{-2} \text{ s}^{-1}$ . For this sample on average 240 tracks were reconstructed per event. The average time taken to reconstruct all track segments in the VELO is about 3 ms per event. A software based implementation of the clustering requires approximately 1.6 ms per event<sup>3</sup>. Neither the tracking nor the clustering algorithms have been optimised extensively for speed, therefore future improvements in execution time are expected. Nevertheless the current performance is within the requirements of the upgrade trigger.

#### 4.4 Primary vertex and impact parameter resolutions

Primary vertices are formed using tracks after the full event reconstruction. Figure 27 shows the difference between the true and reconstructed primary vertex (PV) position. The resolution has a strong dependence on the number of tracks in the vertex, as illustrated in Fig. 28.

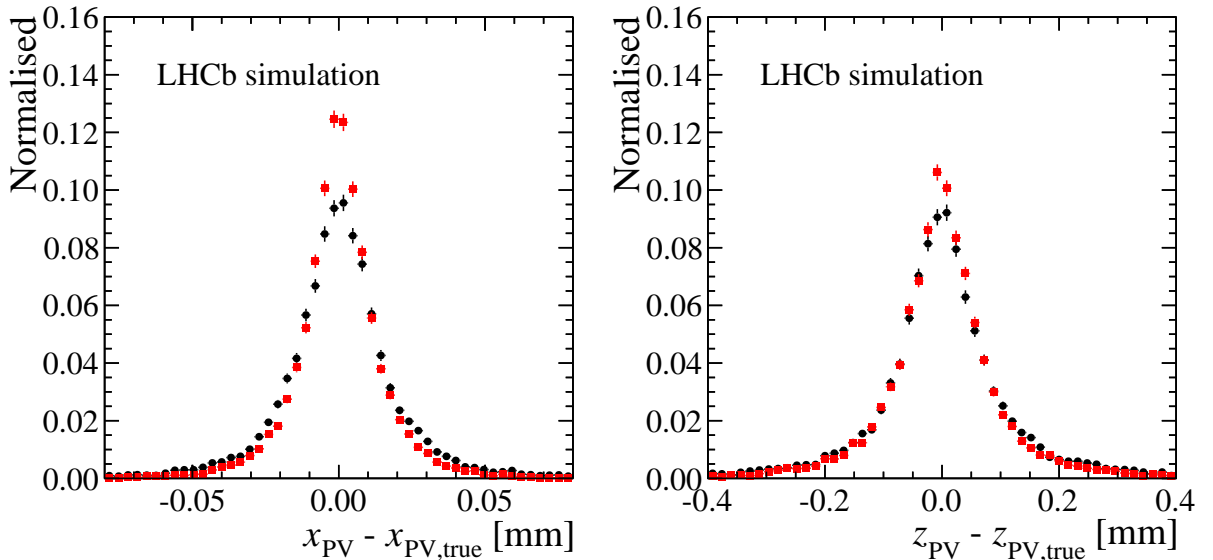


Figure 27: The difference between the true and reconstructed PV position in  $x$  and  $z$  is shown. The current VELO is shown with black circles and the upgrade VELO with red squares, both are evaluated at  $\nu = 7.6$ ,  $\sqrt{s} = 14 \text{ TeV}$ . The resolutions in  $x$  and  $y$  are similar.

The impact parameter (IP) resolution plays an important role in the trigger and in physics analyses. In the latter, impact parameters are used to reduce the combinatorics in searching for partially or fully reconstructed decay vertices. In the following, two types of IP resolution results are presented, (1) those for all track segments reconstructed in the VELO with  $2 < \eta < 5$ , and (2) those obtained for long tracks after the full reconstruction.

<sup>3</sup> These timing numbers were obtained on an Intel Xeon L5520 processor.

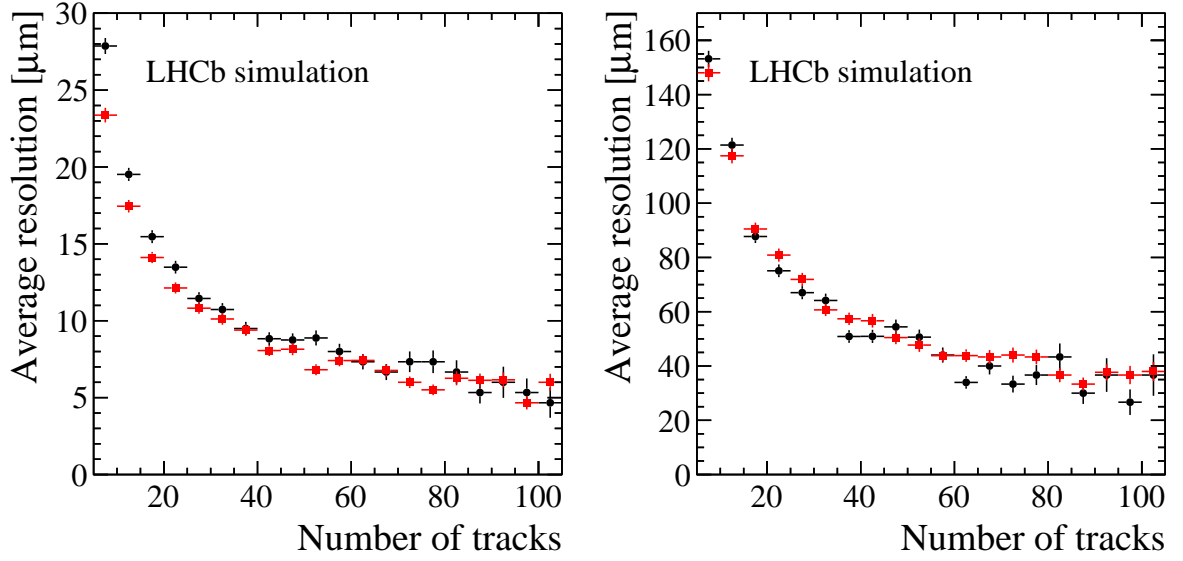


Figure 28: PV resolution in (left)  $x$  and (right)  $z$  as function of the number of reconstructed tracks in the vertex. The current VELO is shown with black circles and the upgrade VELO with red squares, both are evaluated at  $\nu = 7.6$ ,  $\sqrt{s} = 14$  TeV. The resolutions in  $x$  and  $y$  are similar.

The first sample uses only information from the VELO and therefore shows the performance of the VELO independent of any downstream detector, while the latter sample of tracks is used in physics analyses. For simplicity and because the pseudorapidity coverage of current and upgrade VELO is not identical, long tracks are also required to pass the  $\eta$  cut.

Track segments in the first sample are fitted using a Kalman filter, however for VELO track segments no momentum measurement is possible therefore an approximate amount of scattering at fixed  $p_T = 450$  MeV/ $c$  is used in the track fit. For long tracks the momentum measured in the spectrometer together with a map of the material distribution is used in a full Kalman filter track fit.

The impact parameter is traditionally the distance of closest approach between the track and the closest PV. This quantity is also called the “3D impact parameter”. As the distance between a point and a line has two degrees of freedom, the 3D IP does not follow a Gaussian distribution. Therefore, for performance studies the distance vector is often split in two components.

Tracks are locally parameterised by a five-dimensional vector  $(x_0, y_0, t_x, t_y, q/p)$  at given  $z$ -position  $z_0$ . Here  $x_0$  and  $y_0$  are the  $x, y$  coordinates of the track,  $t_{x,y}$  are the slopes and  $q/p$  is the ratio of the charge and momentum of the track. If the PV position is  $(x_{PV}, y_{PV}, z_{PV})$ , then the components of the IP can be defined as

$$\begin{aligned} d_x &= x_0 + (z_{PV} - z_0)t_x - x_{PV}, \\ d_y &= y_0 + (z_{PV} - z_0)t_y - y_{PV}. \end{aligned} \tag{3}$$



The 3D distance can be expressed in terms of these quantities as

$$d_{3D} = \sqrt{\frac{d_x^2 + d_y^2}{1 + t_x^2 + t_y^2}}. \quad (4)$$

In order to study the IP resolution the impact parameter is defined as the closest distance of approach of the reconstructed track relative to the true origin vertex. The RMS of this distribution in bins of  $1/p_T$  was used as an estimator for the IP resolution  $\sigma_{IP}$  in  $x$  and  $y$ . For the resolution of the 3D IP the mean of the distribution was used as an estimator.

The IP resolution is traditionally presented as a function of the inverse transverse momentum  $p_T$ . An approximately linear dependence of the resolution on  $1/p_T$  is expected from Eq. 1. A smaller RF foil radius reduces the multiple scattering term  $\sigma_{MS}$ , for all cases where the traversed foil material is not negligible compared to the detector module material.

The extrapolation term  $\sigma_{extrap}$  decreases with decreasing radial distance of the measured points and with increasing distance between the measured points due to the better lever arm. As a result,  $\sigma_{IP}$  is approximately proportional to the radius of the first measured point.

Figure 29 shows the reduction of the first hit radius in the upgrade VELO. This is mostly achieved by moving the active silicon closer to the beam and leads to a large improvement in the IP resolution.

The most relevant differences between the upgrade and current VELO in terms of IP resolution are:

- A smaller RF foil inner radius (3.5 versus 5.5 mm);
- A smaller inner edge distance to the beams for the sensitive part;  $R_{det} \simeq 5.1$  mm (square hole) versus 8.2 mm (round hole);
- A coarser inner pitch ( $p = 55 \mu\text{m}$  pixels versus  $40 \mu\text{m}$  strips);
- A smaller Si thickness ( $t_{det} + t_{ASIC} = 0.4$  versus  $t_{det} = 0.6$  mm for an  $R-\phi$  station);
- A smaller  $z$  distance between stations ( $\Delta z = 25$  versus 30 mm).

Figure 30 shows the  $d_x$  and  $d_{3D}$  resolution as a function of  $1/p_T$  for the upgraded VELO using all track segments reconstructed in the VELO. Only segments originating from a primary vertex and with pseudorapidity  $2 < \eta < 5$  as determined from truth information were selected. Furthermore the track's origin vertex as determined from truth information was used to compute the impact parameters (the PV reconstruction was not used). The resolutions in  $x$  and  $y$  are approximately equal, but not entirely, due to correlations between azimuthal acceptance and momentum.

To illustrate the performance for tracks as used in physics analyses, Fig. 31 shows the IP resolution for long tracks. As for the VELO track segments the tracks are fitted with

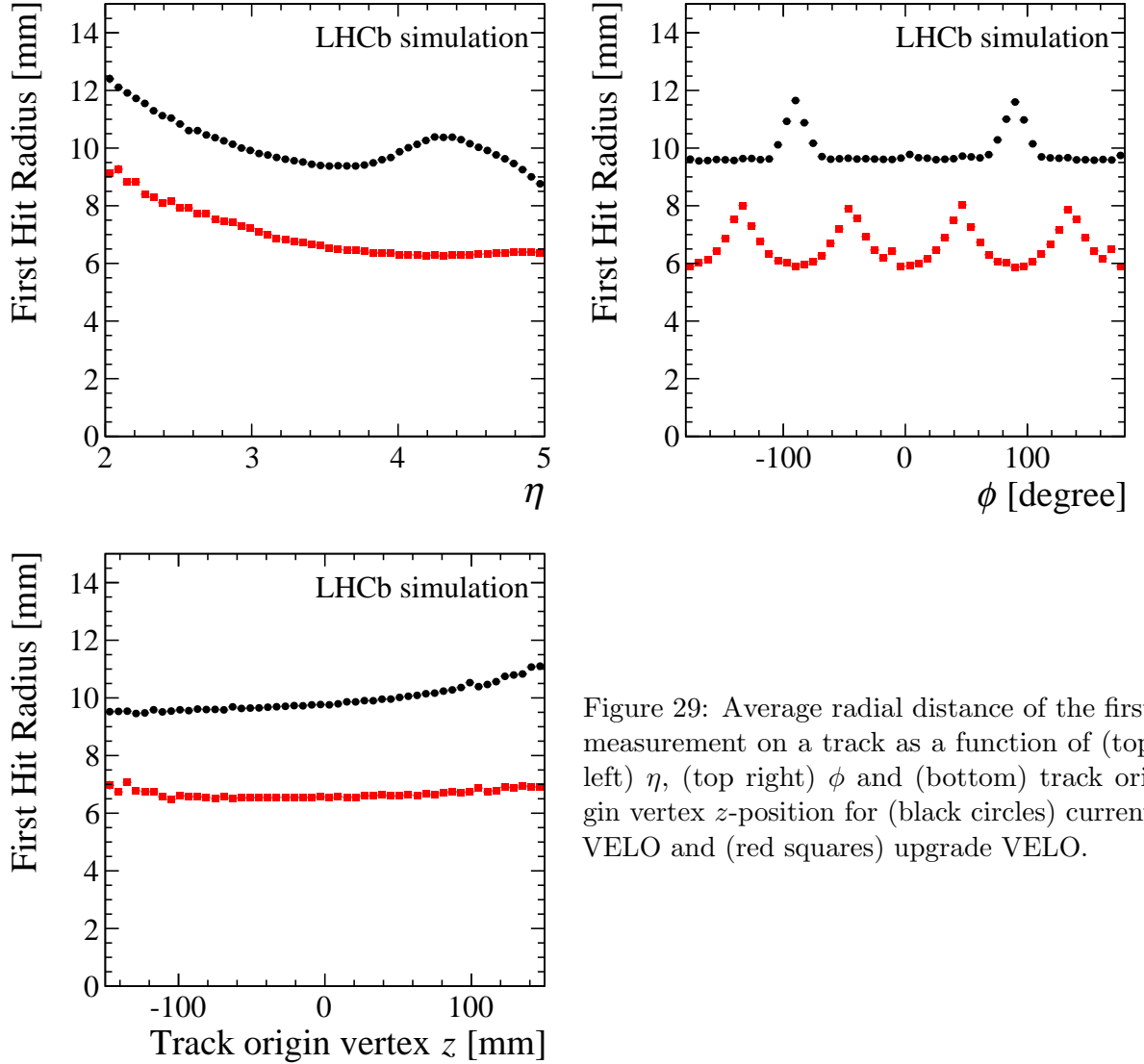


Figure 29: Average radial distance of the first measurement on a track as a function of (top left)  $\eta$ , (top right)  $\phi$  and (bottom) track origin vertex  $z$ -position for (black circles) current VELO and (red squares) upgrade VELO.

a Kalman filter. By using the momentum measurement of the spectrometer instead of assuming a fixed momentum and using a map of the material the resolution is improved compared to VELO tracks. The improvement is largest for high momentum tracks as the fit with a fixed  $p_T$  over estimates the amount of scattering.

The IP resolution distributions are fitted with straight lines corresponding to Eq. 1. The fitted offset and slope for each are given in Table 6.

This confirms our expectation from Eq. 1 about the IP resolution improvements. The intercept value at large  $p_T$  is sensitive mostly to the inner strip pitch and radius. The value is about the same for the upgrade VELO when compared to the current VELO, which corresponds to the fact that their ratio of the quantity  $R_{\text{det}} p / \Delta z$  is very similar, if one uses an effective inner radius of  $1.122 \cdot 5.1$  mm for the square hole to take into account the azimuthal angle dependence of the inner radius.

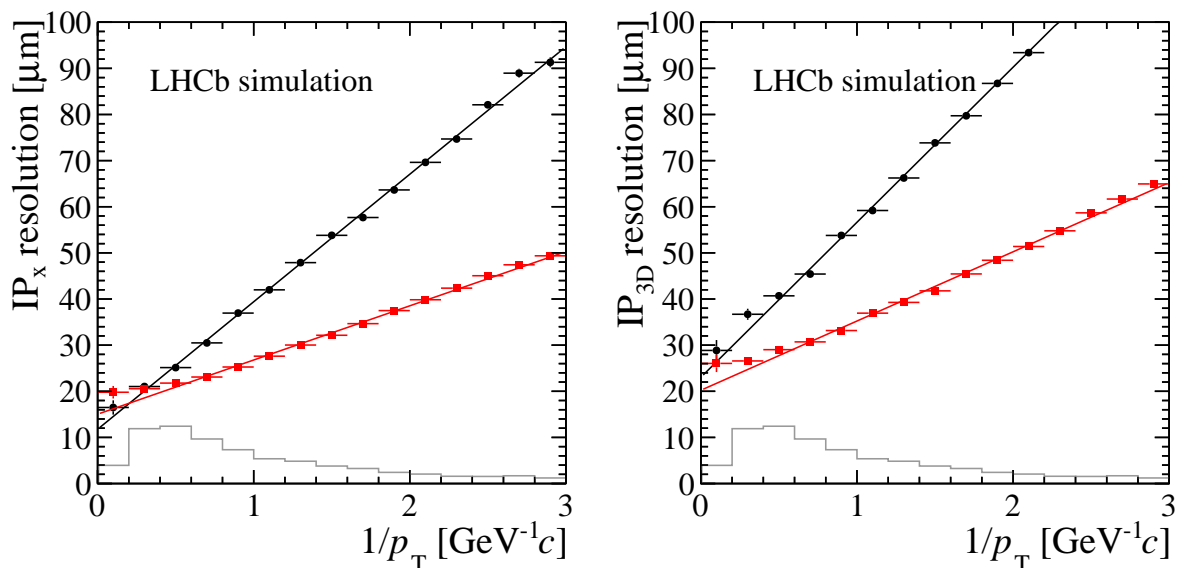


Figure 30: The left figure shows the  $x$  resolution and the right figure shows the 3D resolution of the IP. For both VELO segments with  $2 < \eta < 5$  from a primary vertex are used. The segments were fitted with a Kalman filter using an approximation of the amount of scattering at a fixed  $p_T$ . The current VELO is shown with black circles and the upgrade VELO with red squares, both are evaluated at  $\nu = 7.6$ ,  $\sqrt{s} = 14$  TeV. The resolutions in  $x$  and  $y$  are similar. The light grey histogram shows the relative population of  $b$ -hadron daughter tracks in each  $1/p_T$  bin.

Table 6: Parameters of a straight line fit to the IP resolution distributions in Figs. 30 and 31. For long tracks the measured momentum is taken into account during the track fit. As a result both the offset and slope are improved compared to VELO only track segments for which no momentum estimate is available.

	Offset [ $\mu\text{m}$ ]	Slope [ $\mu\text{m GeV}/c$ ]
VELO only $\sigma_x$	15.0	11.7
VELO only $\sigma_{\text{IP3D}}$	20.2	15.0
Long track $\sigma_x$	11.0	13.1
Long track $\sigma_{\text{IP3D}}$	15.7	16.5

The slope away from the intercept is sensitive mostly to the multiple scattering term. For equal RF foil thickness (0.25 mm) the upgrade VELO slope becomes about 60% that of the current VELO. In agreement with the ratio of their inner edge distance  $R_{\text{det}}$  (the silicon material difference also plays a role and makes the ratio somewhat smaller than  $1.122 \cdot 5.1 \text{ mm}/8.2 \text{ mm}$ ).

Possible improvements in IP resolution performance with different foil geometries were explored. The foil thickness was varied from 0.25 mm to 0 mm in steps of 0.083 mm to show the residual effect of the foil material. Figure 32 shows  $\sigma_{\text{IP}}$  for the different foil

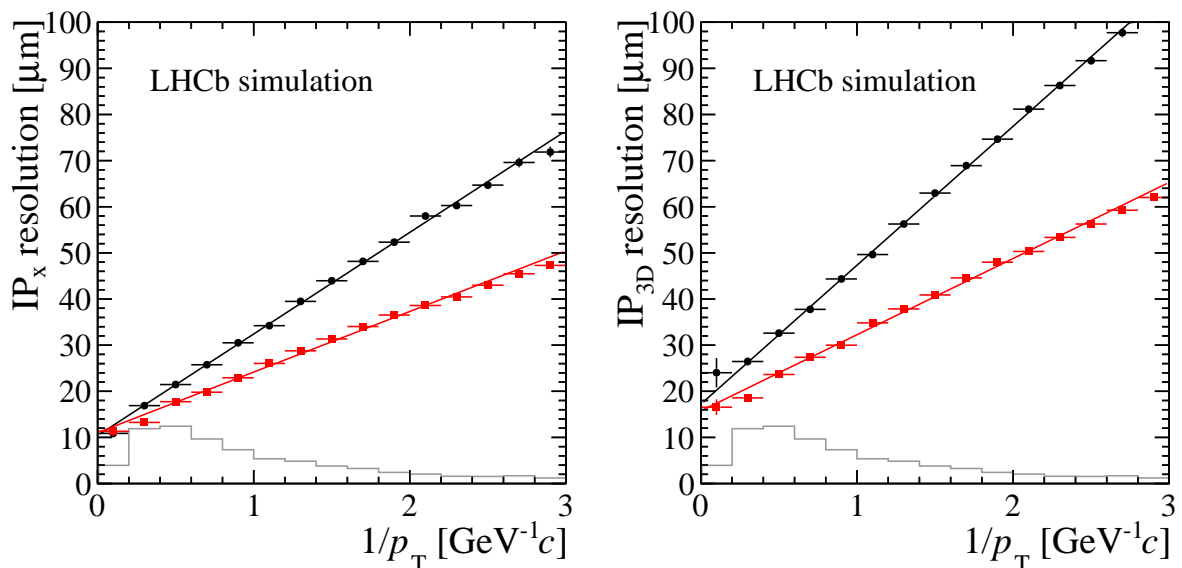


Figure 31: The left figure shows the  $x$  resolution and the right figure shows the 3D resolution of the IP. Long tracks with  $2 < \eta < 5$  from a primary vertex are used for both. The tracks were fitted with a Kalman filter using the momentum measured in the spectrometer. The current VELO is shown in black circles and the upgrade VELO in red squares, both are evaluated at  $\nu = 7.6$ ,  $\sqrt{s} = 14$  TeV. The resolutions in  $x$  and  $y$  are similar. The light grey histogram shows the relative population of  $b$ -hadron daughter tracks in each  $1/p_T$  bin.

thicknesses.

The four different RF foil thicknesses make no difference for the upgrade VELO model at large  $p_T$ . The slopes for the different thicknesses (0 mm to 0.25 mm) of the upgrade models should roughly scale with the square root of the amount of traversed material before the first measured point, this includes the RF foil and the first station silicon. This depends on the average impact angles on the foil and silicon.

## 4.5 Decay time resolution

The most stringent requirement for the vertex resolution is that it is sufficiently good to resolve  $B_s^0$  meson oscillations. For a Gaussian decay time resolution  $\sigma_t$  the dilution on the amplitude of an oscillation with frequency  $\Delta m$  can be written as [9]

$$D = \exp \left( -\sigma_t^2 \Delta m^2 / 2 \right). \quad (5)$$

The current resolution for a benchmark channel such as  $B_s \rightarrow J/\psi \phi$  is about 50 fs which, with a mixing frequency of  $\sim 17.7 \text{ ps}^{-1}$  [10], leads to a dilution of  $\sim 0.7$ . This should be interpreted as an effective loss in the statistical uncertainty on an asymmetry of 30%, or an effective loss in efficiency of 50%. As the dilution drops quickly with worse resolution, the resolution of the upgraded detector should not be worse than that of the current VELO. Figure 33 shows distributions for the error on the  $z$  of the  $B$  vertex and on the decay time

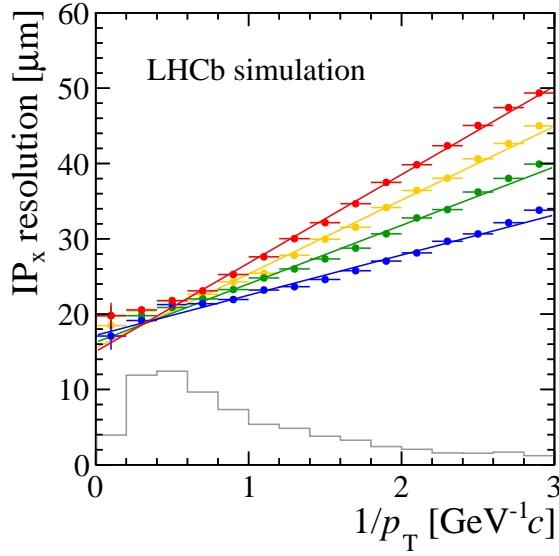


Figure 32: Impact parameter resolution in  $x$  (red) for the upgrade VELO. The nominal thickness of the RF foil is 0.25 mm. Three additional RF foil thicknesses (0.167, 0.083 and 0 mm) are shown in orange, green and blue respectively. The light grey histogram shows the relative population of  $b$ -hadron daughter tracks in each  $1/p_T$  bin.

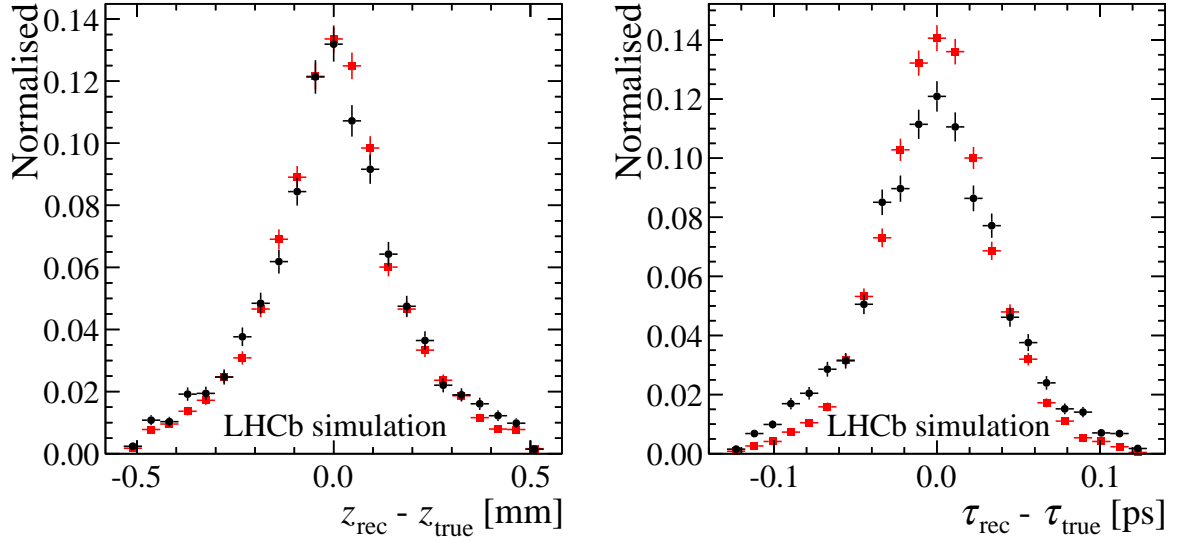


Figure 33: Distributions for the error on the  $z$  of the  $B$  vertex and on the decay time for simulated  $B^0 \rightarrow K^{*0} \mu^+ \mu^-$  decays for (black) current and (red) upgrade VELO at upgrade conditions ( $\nu = 7.6$ ,  $\sqrt{s} = 14$  TeV).

for  $B^0 \rightarrow K^{*0} \mu^+ \mu^-$  decays. Table 7 shows the decay time resolution extracted from the distribution in the figure, both for  $B^0 \rightarrow K^{*0} \mu^+ \mu^-$  and for  $B_s^0 \rightarrow \phi \phi$ . The differences in impact parameter resolution are reflected in the decay time resolution. An improvement of the resolution from 48.3 fs to 43.4 fs changes the dilution from 0.69 to 0.74, corresponding to an improvement in statistical uncertainty of 19% for decay time dependent physics analyses in the  $B_s^0$  system.

Table 7: Decay time resolution (in fs) in simulated events.

	$B_s^0 \rightarrow \phi\phi$	$B^0 \rightarrow K^{*0}\mu^+\mu^-$
Current VELO	$48.3 \pm 0.5$	$41.2 \pm 0.5$
Upgraded VELO	$43.4 \pm 1.6$	$35.3 \pm 0.3$

## 4.6 Performance after irradiation

The expected fluence distribution for the upgrade VELO is given in Sect. 2.1. The maximum fluence after  $50 \text{ fb}^{-1}$  as a function of module  $z$ -position is shown in Fig. 34 (left). The fluence distribution across each module varies significantly, as does the distribution of hits. Figure 34 (right) shows the fluence encountered globally at each hit position, at the end of lifetime of the upgraded experiment. The fraction of hits which occur in regions with a total fluence  $> 2 \times 10^{15} \text{ 1 MeV n}_{\text{eq}}/\text{cm}^2$  is around 27%, while the fraction of hits in regions with total fluence  $> 5 \times 10^{15} \text{ 1 MeV n}_{\text{eq}}/\text{cm}^2$  is less than 5%.

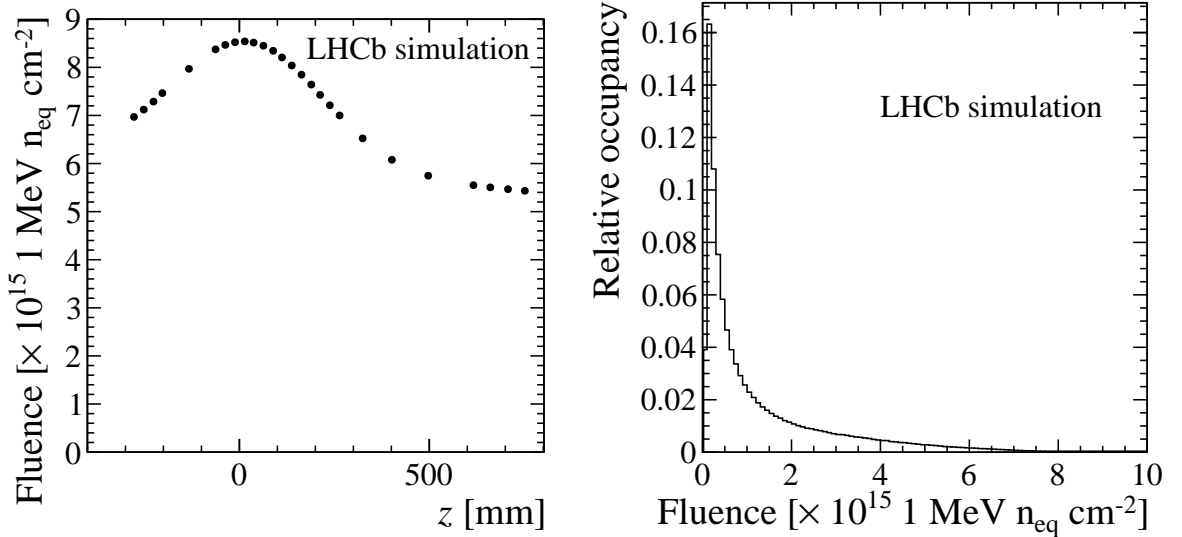


Figure 34: (left) Maximum fluence for each VELO station  $z$ -position after  $50 \text{ fb}^{-1}$ . (right) Fluence distribution for all track intercepts in the upgraded VELO after  $50 \text{ fb}^{-1}$ .

In order to estimate the relative performance after irradiation without an in-depth modelling of the physical processes involved, a simple model was created based on the literature detailing the charge collection efficiency (CCE) of irradiated silicon detectors [11]. For a single sensor thickness, the CCE curve is fitted with a curve of the form

$$a\sqrt{V_{\text{bias}} + b},$$

where  $a, b$  are constants and  $V_{\text{bias}}$  is the sensor bias voltage. Implicitly this contains the assumption that the amount of charge collected is directly related to the depletion depth,

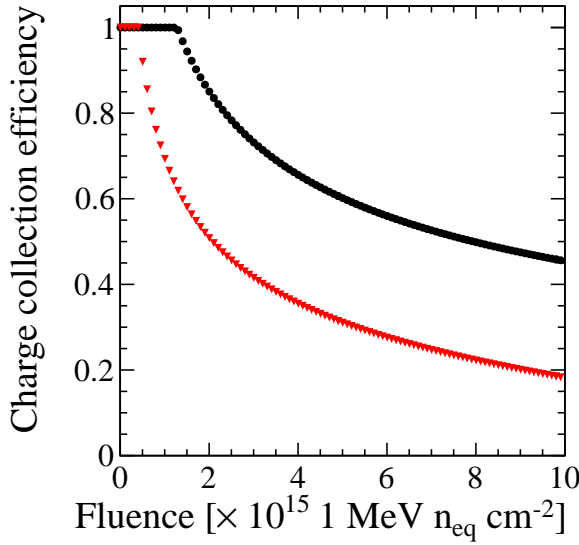


Figure 35: Expected CCE as a function of fluence for a 200  $\mu\text{m}$  thick sensor, for operation at (circles) 1000 V and (triangles) 500 V.

and hence the effects of charge multiplication are ignored. The expected CCE for a 200  $\mu\text{m}$  thick sensor is shown in Fig. 35.

The implementation of this model in the simulation is through a scaling of the active substrate thickness, such that the fraction of active silicon is equal to the predicted CCE. This was taken as a deliberately pessimistic model, which aside from emulating the loss of charge collected would accentuate other features of radiation damage; such as changes to the observed cluster size and the difference in sensor response as a function of depth. Simulations were performed assuming an increase in bias voltage to either 500 V or 1000 V for the duration of the detector operation, with an unaltered pixel threshold of 1000 electrons.

Using this model key performance measures of the VELO are evaluated at different stages of its expected lifetime. Figure 36 shows the single hit resolution, at both 500 V and 1000 V operation voltages, at several intervals between initial installation and final data taking. The plots show the resolution in  $x$  versus the projected track angle  $\theta_x$ , for tracks with  $|\theta_y| < 2^\circ$ . As the detector is read out with a binary ASIC, the effects of reduced charge diffusion are to some extent mitigated, and the most drastic change in resolution is due to pixels which remain below threshold in the more heavily irradiated regions.

Due to the redundancy in tracking stations and the highly non-uniform dose, the tracking efficiencies are robust, as demonstrated in Fig. 37. The efficiencies are determined with respect to the number of reconstructible tracks before irradiation, and a loss in number of reconstructible tracks of  $< 0.03\%$  is observed. The IP resolutions at 500 V and 1000 V are shown in Fig. 38. The loss of hits in the more heavily irradiated regions close to the interaction point leads to a degradation in performance, though as high single hit efficiencies are maintained the overall changes are not extensive.

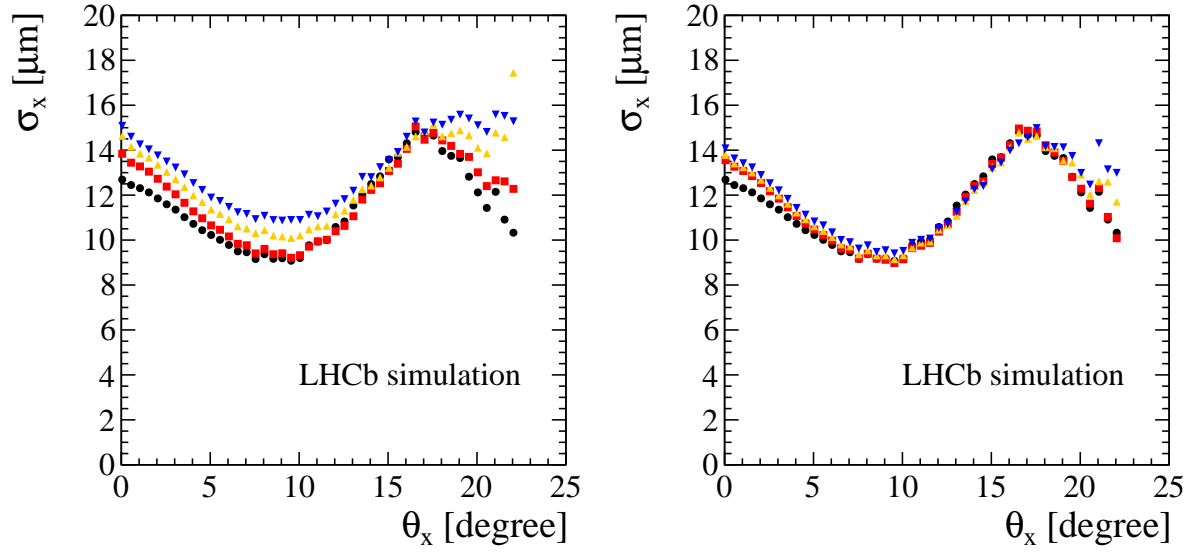


Figure 36: Hit resolution in  $x$  versus projected track angle  $\theta_x$  for the upgraded VELO, shown for (left) 500 V and (right) 1000 V, after (circles) 0, (squares) 10, (triangles) 30 and (inverted triangles) 50  $\text{fb}^{-1}$ . Shown for tracks with  $|\theta_y| < 2^\circ$ .

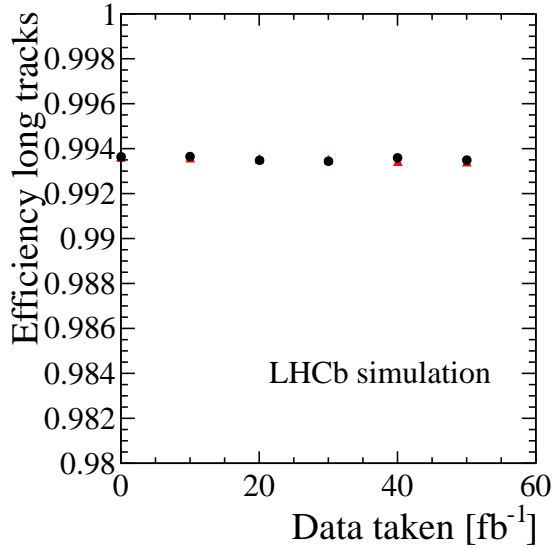


Figure 37: VELO track reconstruction efficiency for particles reconstructible as long tracks versus total integrated luminosity. The data points at (circles) 1000 V and (triangles) 500 V bias overlap.



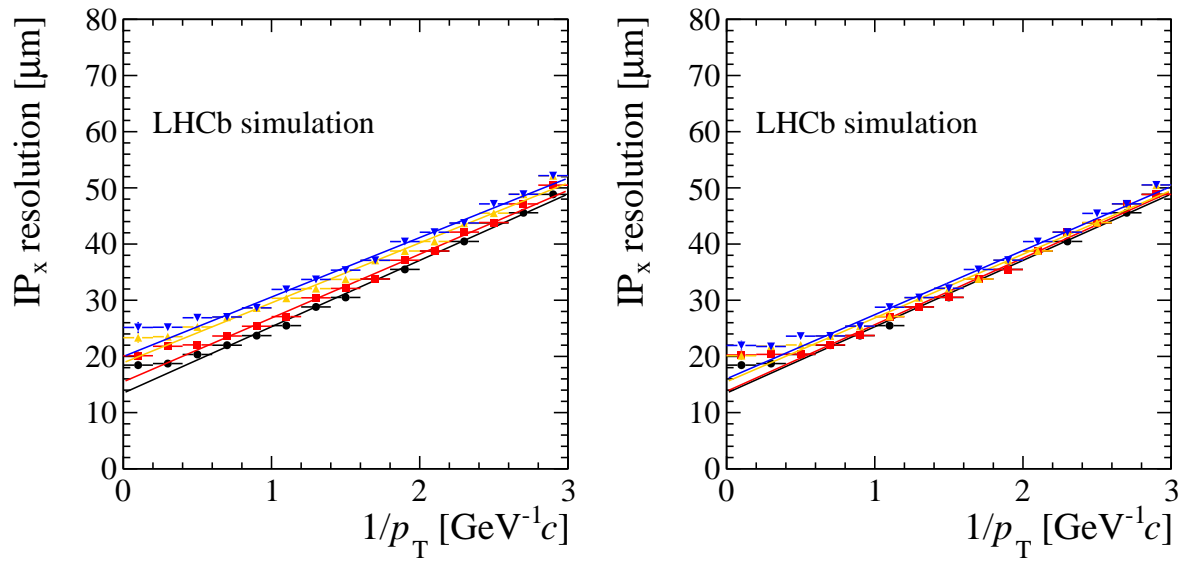


Figure 38: IP resolution in  $x$  for the upgraded VELO, shown for (left) 500 V and (right) 1000 V, after (circles) 0, (squares) 10, (triangles) 30 and (inverted triangles) 50  $\text{fb}^{-1}$ .

## 5 Module

### 5.1 Module specifications, design considerations and layout

A VELO pixel module contains twelve VeloPix ASICs, each featuring a matrix of  $256 \times 256$  square pixels ( $55 \mu\text{m}$  per side), resulting in a sensitive area of  $14.08 \times 14.08 \text{ mm}^2$ . Three chips are grouped in a row and bump bonded to a single sensor to form a tile. Subsequently four tiles are arranged in an “L” shape around the LHCb beam pipe, see Fig. 39. Two silicon sensors are mounted on each side of the module, thus ensuring full coverage in the inner region, a reasonable balance of heat load for mechanical stability, and allowing for electrical connections to the innermost ASICs. The VeloPix ASICs have very slim edges along three sides, and the sensors are fully efficient within the guard ring (GR) area by virtue of elongated pixel implants between the ASIC boundaries.

An important module requirement is that clean measurements of the first points on the track and the most precise extrapolation to the primary and secondary vertices are obtained. The cooling of the tile is supplied by a microchannel substrate onto which the tiles are glued, see Fig. 39. However, the part of the silicon sensors close to the beam axis is most vulnerable to thermal runaway. A compromise is needed between the thermal performance and the minimisation of the material at the tip of the sensors. A compromise was found by requiring that the first measurement point has only a contribution from the material of the sensors and the readout ASICs. This resulted in a configuration in which the tile protrudes the substrate by 5 mm, as represented by the yellow areas in Fig. 39.

Two tiles are glued on each side of the module substrate. The tiles are mounted at right angles such that one tile is read out in the  $x$ -direction and the other in the  $y$ -direction. This results in the readout columns of the chips pointing towards the beam hole, instead of being laterally exposed. This configuration is chosen in order to obtain a lower maximal column hit occupancy and, as a consequence, a more uniform data rate in the columns.

To avoid loss of angled tracks, the sensors on one side have to form an overlap with the sensors on the other side. This displacement amounts to two pixels ( $110 \mu\text{m}$ ) and is determined by the thickness of the substrate ( $0.4 \text{ mm}$ ) and that of the ASICs (twice  $0.2 \text{ mm}$ ).

The drawing in Fig. 39 (right) shows that on that side of the substrate the two tiles are positioned close to each other. This results in a small gap in the acceptance in the outer part of the transverse plane as shown in Fig. 40. The dimension of this gap is determined by the size of the inactive edge of the sensors and the spacing between them. However, there is a full coverage in the inner part, which is essential for an optimal impact parameter resolution.

### 5.2 Sensors

#### Pixel sensor geometry

The chosen sensor geometry causes the following constraints:

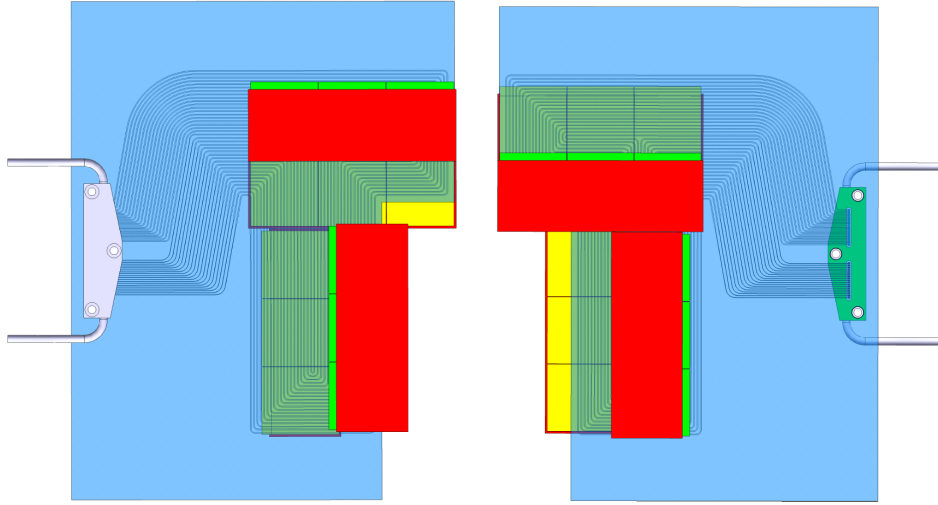


Figure 39: Front and rear side of a module containing two  $3 \times 1$  tiles on either side. Sensors are drawn in red and the microchannel cooling substrate in blue. The bottom sides of the ASICs are drawn in yellow, while the area where the bond pads are located is made green. The overall horizontal and vertical dimensions of the substrate are 80 and 104 mm, respectively.

- The adjacent ASICs need a minimum separation distance to allow for the dicing

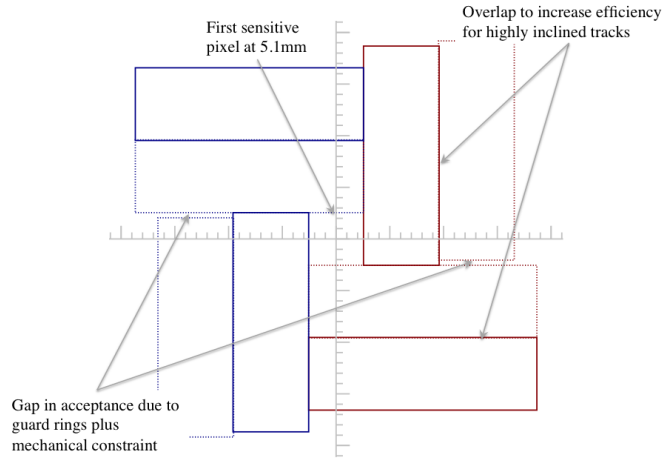


Figure 40: Front  $(x,y)$  view where a module of each detector half is depicted, *i.e.* they are at different  $z$ -positions. The contours of the tiles on the front (back) side of the module of the left half are drawn in solid (dotted) blue. Those of the module on the right half in red. In each module a small gap in the acceptance is visible in the horizontal plane. Tiles on opposite sides of the module are shifted to eliminate a gap for highly inclined tracks.

uncertainties of the chip external border (about  $30\text{ }\mu\text{m}$ ) and the space needed by the bump bonding vendor to align the ASICs to the sensor (about  $50\text{ }\mu\text{m}$ ).

- Although the small inefficient region mentioned above is not critical for the VELO tracking efficiency, an effort to minimise its width is anticipated in the design and prototyping phase. This has also the beneficial effect of reducing the dead area of the sensor in the proximity of the interaction region.

The separation distance between ASICs (inter-chip pixel design) corresponds to twice the inter-pixel pitch ( $110\text{ }\mu\text{m}$ ) to safely take into account the uncertainties mentioned above. Figure 41 shows the inter-chip area of a tile.

The baseline design for the inactive area, which includes implanted guard rings and bare silicon between the active region and the dicing line (called “edge width”), is currently  $450\text{ }\mu\text{m}$ .

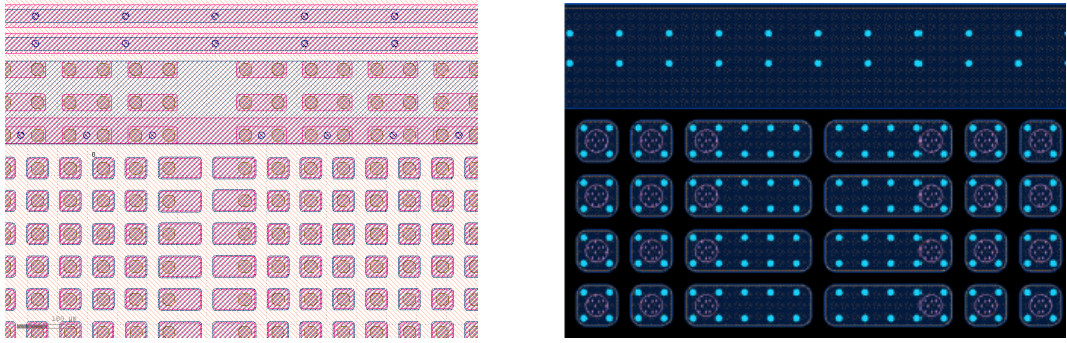


Figure 41: Sensor layout of inter-chip areas implemented in two submissions with Micron Semiconductor (left) and CNM (right). The elongated pixels bridge the area underneath the edges and the separation between two adjacent ASICs. The left example is the minimum distance anticipated for the VELO tile assemblies ( $110\text{ }\mu\text{m}$ , or twice the nominal pitch).

## Radiation tolerance and sensor thickness

One of the main drivers for the detector design is the required radiation tolerance. The detectors will have to withstand a maximum hadron fluence of about  $8 \times 10^{15} \text{ 1 MeV n}_{\text{eq}}/\text{cm}^2$ , at the innermost tip of the sensors. A factor of 40 lower fluence is expected at the opposite side, *i.e.* at the outermost radius of about 4 cm from the interaction point. The combination of the very high maximum dose and the inhomogeneous irradiation are challenging for the detector design, leading to implementation of a radiation tolerant design. For instance via n-side readout to provide the high electric field region near the readout electrodes (pixel implants) after irradiation [12–16]. N-side readout can be realised on n-type (n-in-n) or p-type (n-in-p) silicon bulk with different solutions for the guard rings. The high fluence significantly reduces the signal due to the trapping of the charge carriers at radiation induced trapping centres. This charge deficiency is mitigated by the application of high

electric field on the readout side (hence the advantage of using n-side readout). Figure 42 shows examples of signal degradation as a function of fluence, offering evidence that a good signal can be recovered with the application of sufficiently high bias voltages. This signal is sufficient for fully efficient tracking, considering the low noise and low threshold operations anticipated with the VeloPix ASIC. Moreover after irradiation, the response of the sensors at a given bias voltage depends on the thickness. Figure 43 shows the changes of the signal as a function of fluence for devices of various thicknesses, where it is evident that thinner sensors have a higher charge collection for a given voltage. It can be seen that 140(300)  $\mu\text{m}$  thick detectors collect a signal of 12k(24k)  $e^-$  before irradiation which degrades to 8k(6k)  $e^-$  at 1000 V bias after  $1 \times 10^{16}$  1 MeV  $n_{\text{eq}}/\text{cm}^2$ . The estimated noise for pixel sensors is 160 electrons RMS after irradiation, assuming a conservative equivalent noise charge (ENC) of 150  $e^-$  (including threshold variations) before irradiation. At the estimated operational threshold of  $\approx 1000 e^-$ , this will lead to noise occupancies of  $\leq 10^{-5}$ . Both thicknesses appear to deliver adequate signal over threshold (S/T) values through the entire experimental lifetime. However, a few arguments can be brought forward in favour of the thinner detector option: reduction of the material budget, lower bias voltage during the whole operation time and the possibility of a narrower detector edge (the edge distance needs to be larger than the thickness; therefore thinner detectors can operate with narrower edges). In practice, the lower limit on the thickness is set by the mechanical handling, and higher chances on high yield in the bump bonding process. These results suggest the choice of thinner sensors, with respect to the standard 300  $\mu\text{m}$  thick option currently installed in the VELO. A thickness of 200  $\mu\text{m}$  seems optimal.

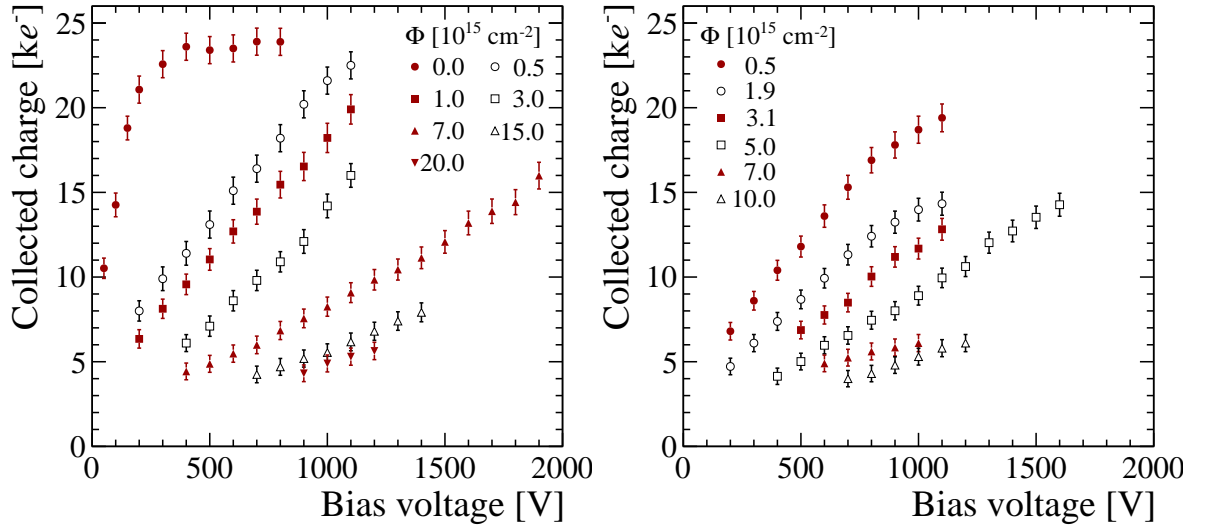


Figure 42: Degradation of the collected cluster charge as a function of bias voltage measured with 300  $\mu\text{m}$  thick sensors irradiated to various fluences  $\Phi$  of reactor neutrons (left) and 24 GeV/c protons (right). It is noticeable that the sensors can be biased to very high voltage after irradiation. Reproduced from Ref. [16].

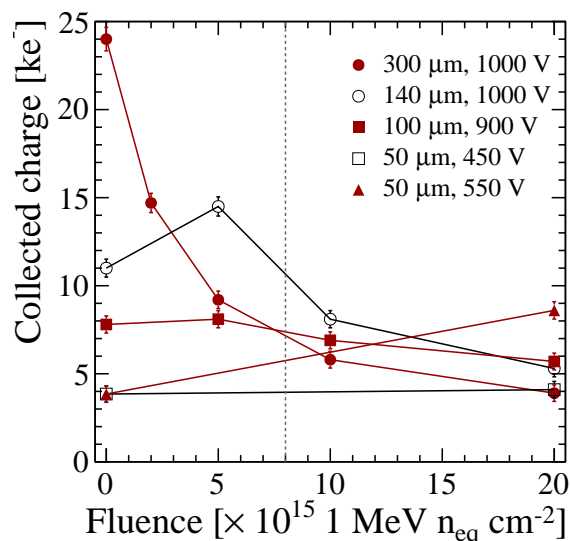


Figure 43: Degradation of the signal with fluence for detectors with different thicknesses. The vertical line corresponds to the expected maximum hadron fluence of  $8 \times 10^{15} \text{ 1 MeV } n_{\text{eq}}/\text{cm}^2$ .

### Bias (HV) voltage specifications

As above indicated, the VELO sensors will have to be operated at high bias voltage after severe irradiation, while before irradiation an over-bias with respect to full depletion voltage is required. Highly irradiated silicon sensors can typically sustain very high bias voltages with no breakdown, as shown in Fig. 43. However, because of the radial dependence of the irradiation in the VELO, the innermost region will require a high bias voltage after irradiation, while at the same time the outer region, with a factor 40 lower fluence, should sustain this voltage with no breakdown. The selection procedure for the VELO sensors will have to take into account this particular feature and being able to assure the performance of the sensors during the whole physics data taking period. Also, the radiation induced changes in the sensors lead to different biasing needs depending on the choice for n-in-n or n-in-p. In the first case, the bulk will undergo type inversion from n-type to effective p-type after a fluence of some  $10^{13} \text{ 1 MeV } n_{\text{eq}}/\text{cm}^2$ . At this dose the required bias voltage can be as low as a few tens of Volts. With a difference of forty times in fluence, another area of the sensor might require a bias voltage of a few hundred Volts. Reverse current measurements before irradiation are part of the quality assessment procedure. The irradiation programme will have to prove that this particular situation on the sensor is well tolerated and operations are not compromised. In the case of p-type bulk, the reduction of the operation voltage with fluence is much less pronounced. Therefore, with the choice of a relatively low initial p-bulk resistivity (to yield a full depletion voltage between 150-200 V) the difference between the operation voltages between the two opposite tips of the sensor can be reduced.

Initial specification of a high breakdown voltage before irradiation ( $> 500 \text{ V}$ ) for  $200 \mu\text{m}$  thick detectors and with full depletion voltage between 50 to 200 V for a n-type bulk and between 150 to 250 V for p-type bulk are presently foreseen, but subject to confirmation by the irradiation program.

To guarantee there is some headroom during the full lifetime of the detector the requirement is put that the sensors should be able to sustain 1000 V.

### Edge spark protection

In hybrid pixel assemblies the distance between the edge of the sensor and the edge of the ASIC is in general between ten to twenty microns. The edge of the silicon sensor can sit at high voltage, while the ASIC is at ground potential. In some cases this has lead to sparking electrical discharges with unrecoverable damage to the assembly [17]. This effect depends on the assembly, but safety measures should be taken to prevent possible sparking when high bias voltage is needed for adequate charge collection (e.g. after irradiation). Several methods are envisaged: benzocyclobutene (BCB) or parylene edge coating or adequate implant structures to reduce the edge potential (e.g. backplane GRs). Typically, the coating methods are executed as a post-processing step (after bump bonding of the assembly) and can be performed on any type of geometry.

### Guard ring design

The application of high bias voltage to the sensors requires the implementation of protection structures and a bare silicon space surrounding the active area. Some typical protection geometries are shown in Fig. 44 (left).

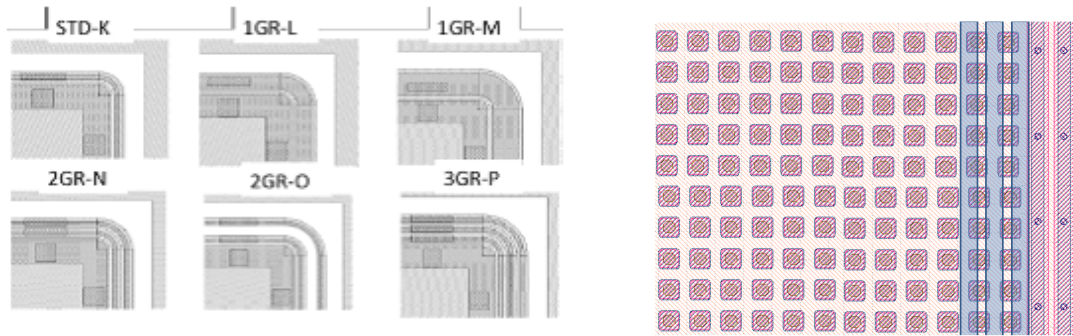


Figure 44: (left) Example of different guard ring designs and bare silicon area between sensitive region and cutting line (together they form the “edge”, or non-sensitive area). (right) Example of displaced backplane GR in n-in-n detectors. The backplane GRs (light blue) are implanted underneath the edge pixels. This solution allows a reduced edge.

In essence, the distance from the active volume to the cut edge is the key parameter for safe operations. Breakdown can occur when the depletion region reaches laterally the cut edge. The voltage at which this happens depends on the distance to the second power and the bulk resistivity (lower resistivity substrates require higher voltage to deplete the sensor up to the edge).

The two possible bulk solutions require a different approach to the GR design. The n-in-n type demands that the GRs are implanted on the backplane of the sensor (where the  $p^+$ -n junction is formed). A series of  $p^+$  rings surrounding the large  $p^+$  diode (as large as the active area of the sensor) are needed. This implies double sided processing with extra cost with respect to the single sided planar technology (e.g. n-in-p type). Nonetheless, the presence of the GRs on the backside can allow for a reduction of the edge distance, if the area of the GRs slightly overlaps the active region. Figure 44 (right) shows this solution. A small distortion of the electric field is expected in the region of pixels overlapping the GR, with a limited impact on the local point resolution.

In the present baseline design, the edge width is  $450\text{ }\mu\text{m}$ , but with the choice of thin devices and optimised GR design we aim to further reduce this distance.

## Results and plans for sensor R&D

Various pixel and microstrip detectors, readout with a variety of ASICs, have been shown to operate with full efficiency to fluences well above the maximum anticipated for the VELO sensors. Sensors made with either n-in-n or n-in-p technologies provide sufficient signal after  $8 \times 10^{15}\text{ }1\text{ MeV n}_{\text{eq}}/\text{cm}^2$  when biased to a voltage between 500 to 1000 V (depending on the thickness). The performances of the VELO sensors have nonetheless to be tested as a function of irradiation mainly due to the radial dependence of the fluence distribution. In particular, the ability to apply the voltage required for full efficient operation of the area more exposed to radiation without incurring in the breakdown of the less irradiated region has to be confirmed by dedicated tests. The main points to be confirmed by tests with VELO sensors are the following:

- Charge collection as a function of bias voltage at various fluences. This test determines the required bias voltage after different operation times in the experiment up to the maximum fluence. Referring to the most exposed (inner) area, test of performance after 0.5, 1, 2, 4 and  $8 \times 10^{15}\text{ }1\text{ MeV n}_{\text{eq}}/\text{cm}^2$  are anticipated. These measurements can be performed with single chip assemblies using laboratory equipment.
- Radiation test of detector tiles irradiated with a fluence distribution similar to the radial dependence found in the actual experiment. These tests will assess the robustness of the high voltage protection against breakdown in realistic conditions. The non-homogeneous irradiation will be performed in dedicated scanning systems available at the CERN-PS, Karlsruhe and Birmingham irradiation facilities. Long term biasing tests after irradiation, carried out in the laboratory, will confirm the ability to apply the required bias voltage.
- Topological characterisation of irradiated detector tiles (full efficiency over the entire area) as a function of fluence. This test requires test beam facilities, which are available at DESY and CERN-SPS.
- Power dissipation (increase of the reverse current) after irradiation.



- Effect of annealing on signal and current. These tests will allow establishing the thermal management strategy of the sensors during beam-off periods. The temperature of the assemblies during operation is determined by the need of limiting the reverse current and preventing thermal runaway, as described in the session dedicated to the cooling system.

In 2014 a short R&D phase is programmed to test the small variations of the geometry of the VELO sensors. The design of a few variants of sensors to explore the optimal design solutions for substrate type, minimal edge distance, adequate HV performance, and optimal thickness and charge collection efficiency after irradiation will be implemented by the interested vendors on a 6 inch prototyping wafer. The various solutions will be implemented in both single devices and three chip tiles. This will allow selecting the optimal sensor design well in time for the final tests with VeloPix electronics.

### 5.3 Tile production

Three ASICs will be bump bonded to a sensor to form a tile. The bumps provide both the electrical and mechanical connection and are a crucial component of the detector assembly. Bump bonding is a technologically challenging step. The procedure has been a cost and schedule driver in previously built pixel detectors.

The challenge that the bump bonding of the VELO upgrade sensors will pose for industry, with respect to their main stream demand, is in the smaller geometrical features which require high placement accuracy of the bonder and smaller bump heights. Also the relatively large size of the sensor, with a high interconnect density, and the slim ASICs can pose problems.

The VeloPix ASICs will be thinned to a thickness of 200  $\mu\text{m}$  to reduce the material budget in the VELO. The thinning of the ASICs might introduce stress to the material that later can cause problems in the bump bonding procedure. The corresponding investigation is part of the process development procedure. Also the handling and placing method of the ASICs during the bonding must be optimized.

A survey of possible bump bonding vendors is still ongoing.

#### Bump bonding process

Each vendor has its own bump bonding process. Differences lie in the materials and chemicals used and even process steps can be performed in a different order. Here we explain the general process of bump bonding, which is a complicated procedure involving many different production steps and high precision handling.

Indium, lead solder and silver solder bumps have all been successfully used in previous built HEP pixel detectors [14, 15, 18]. The main difference between these materials is the reflow temperature.

The full bump bonding process can be divided in three different procedures. The preparations of the ASICs, of the sensors and the flip-chip procedure that connects the two.

For the preparation of both the ASIC and the sensor, first an under-bump metallisation (UBM) step is performed. This step might be performed either by the company producing the sensor/ASIC or by the bump bonding vendor. Usually, this step includes removal of the aluminium oxide layer, the deposit of a non-oxidising conductive layer and photolithographic treatment. The UBM provides a robust mechanical connection between the bumps and the bump pads on the sensor and ASICs. A layer of bump material is put on the sensor, after which in general the photo-resist is lifted off from both the sensor and the ASICs. The sensor is reflowed creating spherical bumps due to the surface tension of the molten bump metal.

Finally, the ASICs and the sensors are joined with a flip-chip procedure to form the tile. Three ASICs are placed on a single sensor with high precision, after which the whole tile is reflowed. The surface tension of the molten bumps provides self alignment of the ASICs with respect to the sensor. After the reflow a good mechanical connection is established.

Small anomalies in the process can have large effects on the quality of the delivered tiles. In order to prevent large losses in production yield, continuous monitoring of the production quality should be performed and quick feedback should be provided to the vendor.

It is possible to develop a rework routine for underperforming tiles. Several groups have developed techniques to lift-off bump bonded ASICs from sensors, either by heating and pulling or by using a diamond saw. The ASIC can be removed in case there are one or more ASICs with low performance, either due to ASICs malfunctioning after the bump bonding procedure or missing or failing bump interconnections. After this fresh ASICs can be placed on the sensor by repeating the flip-chip technique. Such a rework procedure requires the development of special routines, but can still be cost effective depending on the initial and rework success rates.

## 5.4 Hybrid and additional on-board electronics

### Hybrid

Two electrically similar, but geometrically different, multilayer flexible polyimide or liquid crystal polymer (LCP) printed circuit “hybrids” will provide power, high voltage, signal distribution and readout signal routing to two three-chip sensor assemblies and control chips on each side of the module. Details about dimensions and materials are given in Sect. 7.2. These hybrids, complete with passive components and connectors, will be positioned within  $200\text{ }\mu\text{m}$  using jigs or optical alignment from holes or fiducial marks on the hybrid and glued to the two sides of the cooling substrate before attachment of the sensor assemblies (see Fig. 45).

### Wire bonding

The VeloPix chips will protrude from under the sensors and this constrains the bonding direction to be from the chip to the hybrid to avoid the bonder clamps touching the sensor. Normally this would be called “bonding down” but with the VeloPix being thinned to

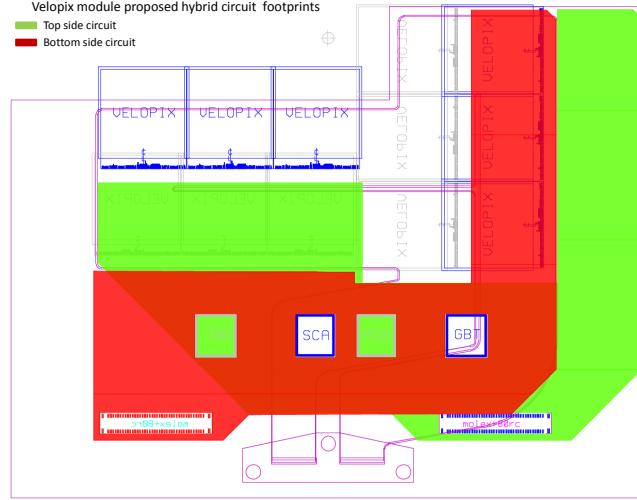


Figure 45: Layout of a module with VeloPix ASICs, and hybrids on either side of the substrate in red and green.

200  $\mu\text{m}$  then the hybrid pads will be up to 150  $\mu\text{m}$  higher than the chip surface. To avoid interference with the bonder clamp, which is only 85  $\mu\text{m}$  higher than the bond foot, the edge of the hybrid must be at least 1 mm away from the chip edge. This will not apply to the SCA, GBTx and GBLD chips (see Sect. 7.1), which will be mounted on the hybrid itself (see Fig. 46).

### Hybrid prototype program

A kapton hybrid, containing two copper layers, is designed for the readout of one, two and three Medipix3 chip tiles. It has been manufactured and tested with two Medipix3 chips and a two-chip sensor. A zoomed view of two chips, wire bonds and hybrid with connectors is shown in Fig. 47.

Power, bias, signal inputs and outputs were provided via a custom 250 mm long kapton cable and adapter cards into a USB readout system. (see Fig. 48)

The long cable makes it possible to place the non-radiation hard voltage regulators and active components remotely, to allow chips to be powered during an irradiation or a beam test. A new design using the 4 layer construction outlined in Sect. 7.2 and suitable for three Timepix3 chips and a three-chip sensor is underway, together with a suitable cable and adapter card to interface to a Fitpix or SPIDR readout system. First parts are estimated to be ready by the end of November and to be available for test beam experiments in February 2014.

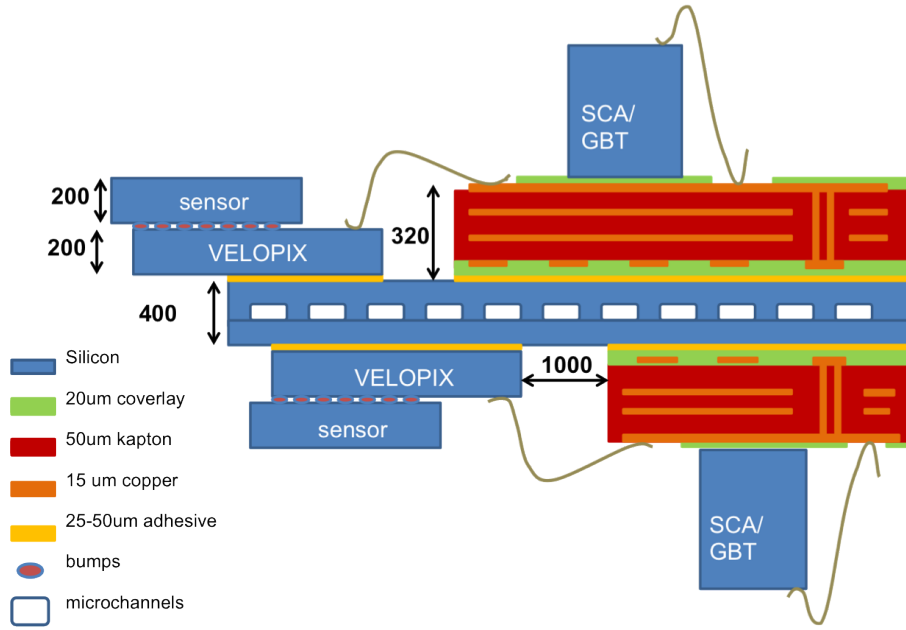


Figure 46: Schematic cross section of a module with sensors, VeloPix chips, SCA/GBTx/GBLD chips, microchannel substrate, hybrids and bond wires (not to scale). Measures are in  $\mu\text{m}$ .

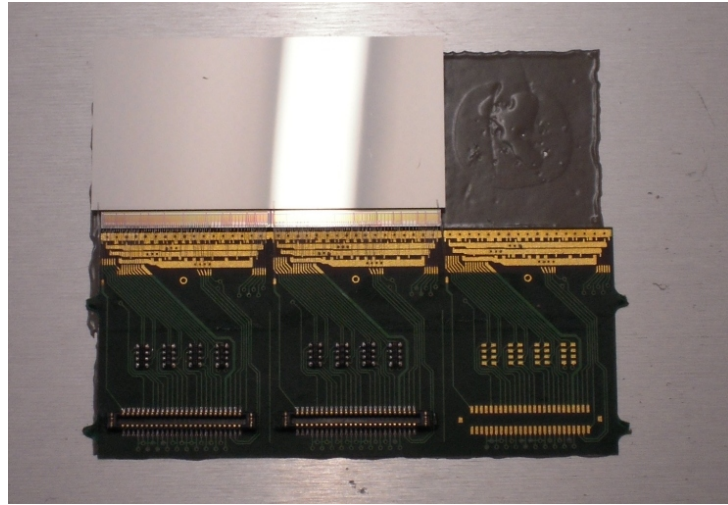


Figure 47: Close-up of a tile consisting of a two-chip sensor bump bonded to two Medipix3 chips, which is wire bonded to a hybrid.

## 5.5 Module pedestal

The substrate with four tiles, two hybrids and a  $\text{CO}_2$  connector with inlet and outlet capillaries is mounted on a module pedestal to form a complete module. This object is

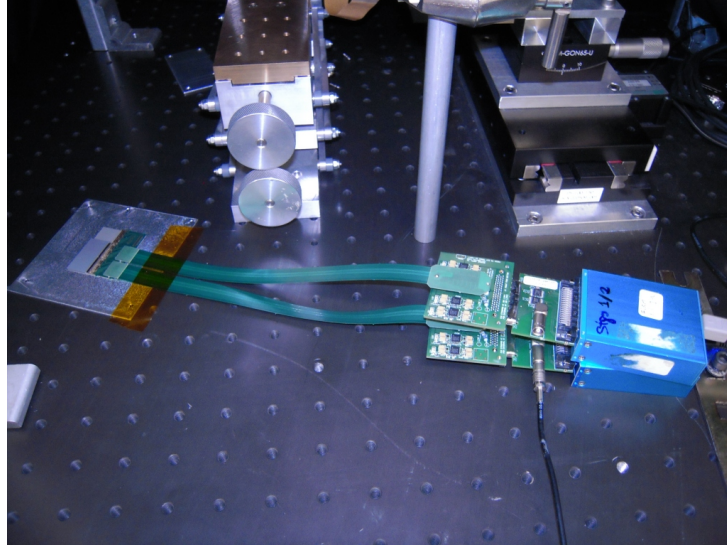


Figure 48: Two-chip tile connected to a USB readout system.

then later mounted on the module base, orbital welded to the CO<sub>2</sub> supply and outlet tubes for cooling and electrically connected via high-speed links.

The foot of the pedestal is likely to be similar to the one of the present VELO: a carbon fibre (CF) structure with on each side an invar piece with a dowel pin for precise positioning. For the connection between substrate and foot two possibilities are under design: one that connects to the CO<sub>2</sub> connector as it represents the most rigid point (see Fig. 49 (left)) and the other that uses two holes in the corners of the substrate (see Fig. 49 (right)). Both use 1 mm thick CF support bars with an outer diameter of 6 mm.

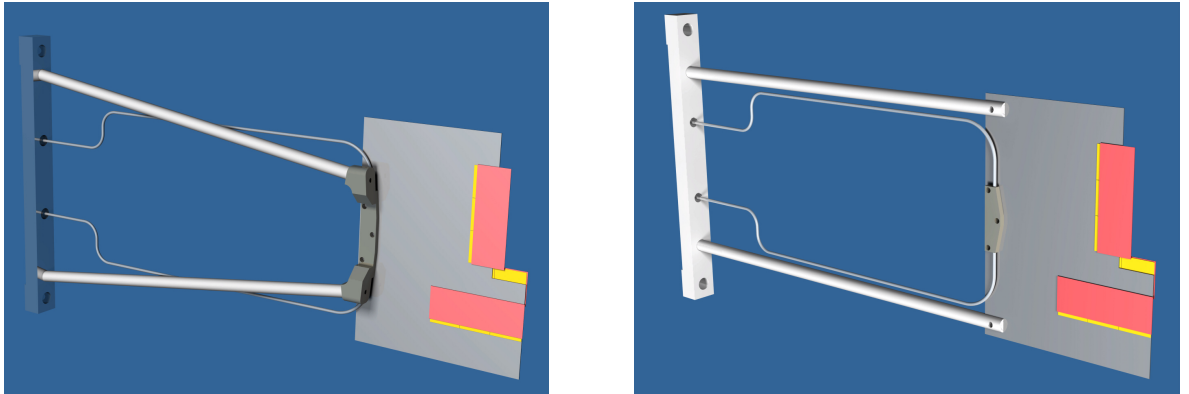


Figure 49: (left) module design in which the CF structure uses the CO<sub>2</sub> connector as point of attachment. (right) module design in which two holes in the substrate are taken as point of attachment.

## 5.6 Module assembly procedures and quality assurance

In other sections the design, construction, production and qualification of the hybrid (Sect. 5.4), tiles (Sect. 5.3), module pedestal (Sect. 5.5), microchannel substrate and CO<sub>2</sub> connector (Sect. 9.6) are described. Here, the assembly of the individual building blocks into qualified full-scale VELO modules, ready to be installed on the module base, is described. Thanks to the modular design and the fact that all VELO modules are identical, we expect to obtain a high yield in the module production step.

To prevent damage of the coated surfaces of the substrate, first the CO<sub>2</sub> connector with welded inlet and outlet capillaries has to be soldered on to the microchannel substrate. Since this is a delicate operation and involves crucial safety issues the combined setup then has to be qualified by means of cooling and pressure tests. The plan is to simultaneously cycle the pressure of the assembly in a vacuum chamber up to 150 bar, while also cycling the temperature between -40 and +40°C.

The hybrid will be equipped with passive Surface Mounted Devices (SMDs) and Molex connectors for both powering and the electronic signals. The gluing of the two hybrids on either side of the substrate is a high-precision job as the smallest wire pad distance of the VeloPix chip will likely amount to  $\approx 100\text{ }\mu\text{m}$  and as such largely determines the lateral position at which the tiles will have to be placed later on. By making use of the markers on the hybrid and the substrate the expected precision with which this can be achieved is estimated at  $100\text{ }\mu\text{m}$ . Due to the fact that the module has to be operated in vacuum special attention has to be paid to the elimination of air bubbles during the gluing procedure.

Next step in the module assembly is the placing of the GBTx, SCA and GBLD chips on the hybrid. The tiles are then mounted with  $\leq 10\text{ }\mu\text{m}$  precision with respect to the fiducial marks on the substrate. The thermal gradients are largely determined by the properties and thickness of the used glue. Two promising options are being investigated. We plan to either use Stycast FT2850 and catalyst 9 with a layer thickness of  $\approx 50\text{ }\mu\text{m}$ , or double-sided adhesive film 9461P from 3M. The latter has a thickness of  $30\text{ }\mu\text{m}$  and has been tested by NA62 for radiation hardness up to  $10^{15}$  neutrons/cm<sup>2</sup>.

Next, the wire bonding between hybrid and ASICs, SCA, GBTx and GBLD chips has to be performed, as well as those of the HV connection. (See Sect. 5.4)

The assembly is then mounted to (part of) the mechanical module support, such that it can be handled more easily. The next step is to verify the HV connections by measuring an IV-curve, followed by a quick electrical test without cooling at room temperature.

If these have given satisfactory results a full-scale test cycle in vacuum can start, during which the module is cooled by CO<sub>2</sub> to the foreseen operational temperature of -30°C. Here, electrical characterisation of the module will be performed, with among others noise maps of all VeloPix chips with and without bias voltage being applied to the sensors. With a thermal camera images of both sides of the module will be recorded in order to check the functioning of the cooling in combination with powering the ASICs. Taking data with test-pulses and a radioactive source are the last two tests to be performed. Once a module has been fully qualified from the electronic point of view, it can mechanically be finalised.

The last step of the module production involves mapping the sensor parts out in 3D by measuring their coordinates with a high-precision metrology device with an accuracy of  $\leq 5\text{ }\mu\text{m}$ .

Burn-in of all modules is the last step in the module construction and quality assurance, before proceeding to the assembly (see Sect. 10.3.1).

All recorded data will be stored in a database, which permits to identify later on trends in specific characteristics.

## 6 VeloPix

### 6.1 Overview

The readout of the pixel sensors is done by VeloPix ASICs which consist of a matrix of  $256 \times 256$  pixels of  $55 \times 55 \mu\text{m}^2$  each. The VeloPix is a binary pixel readout ASIC and features a data driven readout which means that every hit is time-stamped, labeled and immediately sent off chip. The VeloPix ASIC is based on the Timepix3 ASIC, and is also designed in the IBM 130 nm CMOS process. Therefore the Timepix3 can be considered a first full scale prototype. A large number of building blocks from the Timepix3 (and Medipix3) ASIC are reused for the VeloPix. These blocks are amongst others, parts of analog front-end, the digital high density cell library and many peripheral blocks such as DACs. Both ASICs are designed by the same group of people with designers from CERN and Nikhef (and also from Bonn university for the Timepix3). We aim to submit a first version of the VeloPix in Q3 2014. The Timepix3 has been submitted in May this year, and testing has started recently. First test results of this ASIC are described in Sect. 6.5.

The Timepix3 also features a data driven readout, similar to the one required for VeloPix. However, the major difference between VeloPix and Timepix3 is the average hit rate it must handle. One of the challenges of the VeloPix is to collect the pixel hits from the matrix and to send out the data to the DAQ for each bunch crossing, since the ASIC does not feature a triggering scheme. For VeloPix the hit-rate amounts to 600 million pixel hits per second, which is a factor 8 greater than the Timepix3 specification. This increased hit rate translates to an increase of the output bandwidth from 5.12 to an average of (at least) 10.2 Gbit/s. The increase of output bandwidth is smaller than the increase of hit-rate because (i) the amount of information per pixel hit is reduced (binary instead of Time over Threshold readout, coarser timestamp and smaller range) and because (ii) groups of neighbouring hits arriving in the same bunch crossing are packed into so-called super-pixel packets (see next sections for a detailed description). Given the average number of hits in a cluster of 2.2, the packing will reduce the amount of data to be transmitted by 30%, since the redundant timestamp and (pixel) address information are removed. A side effect of the chosen readout structure is that the data is not read out in time order. Time re-ordering of hits therefore has to be done in the TELL40 cards, as will be explained in Sect. 8.

An overview of the ASIC occupancies and rates is given in Table 8. The difference in rate from module to module is modest.

### 6.2 Specifications

In this section the main specifications of the VeloPix ASIC are discussed. Information about the track rates and cluster sizes is obtained from the physics Monte Carlo simulation as described in Sect. 4. Because the VELO modules are placed perpendicularly to the beam, the occupancy from ASIC to ASIC varies by almost a factor 10. This effect is shown in Fig. 50. Since there is only one type of VeloPix ASIC this implies that the ASIC



Table 8: Overview of VELO Upgrade ASIC occupancies and rates.

Mean Cluster Size	2.2 (threshold 500 e <sup>-</sup> )
Mean # tracks / module / event	32.8
Mean # tracks / event, hottest module	35.1
# pixel hits per module / event	69.3
# pixel hits, hottest module	92.0
Hottest ASIC mean output rate	10.2 Gbit/s
Hottest ASIC peak output rate	15.1 Gbit/s
Cooler ASIC mean output rate	0.86 Gbit/s
Cooler ASIC peak output rate	1.28 Gbit/s
Average data rate per module	36.8 Gbit/s
Peak data rate per module	54.7 Gbit/s
Data rate, hottest module	41.2 Gbit/s
Peak data rate, hottest module	61.2 Gbit/s
Total data rate	1.92 Tbit/s
Peak total data rate	2.85 Tbit/s

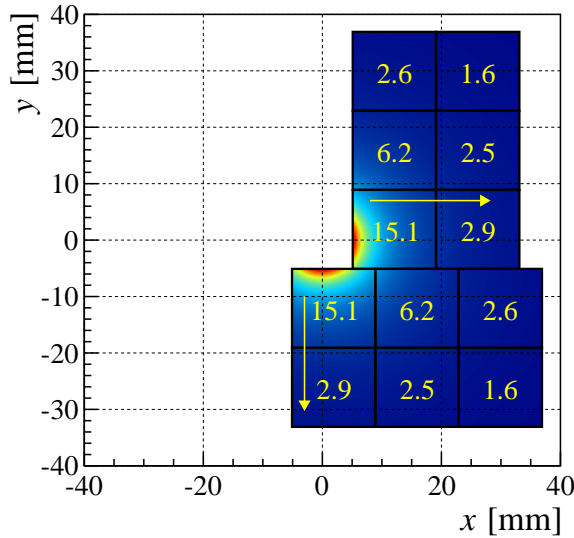


Figure 50: Data rate per ASIC in Gbit/s for the most active module. The readout direction is indicated by arrows.

is designed for the toughest conditions, and hence in the following all specifications are for the most active VeloPix in the VELO.

A summary of the specifications of the VeloPix ASIC is shown in Table 9. For comparison, the specifications of the Timepix3 ASIC are shown as well. The data rate specifications are the minimum the ASIC has to comply with.

The ASIC is designed to cope with a rate corresponding to an average instantaneous luminosity of  $2 \times 10^{33} \text{ cm}^{-2}\text{s}^{-1}$ . For the physics simulations it is assumed that 2400 of the

Table 9: Specifications of the Timepix3 and VeloPix. For the latter a luminosity of  $2 \cdot 10^{33} \text{ cm}^{-2}\text{s}^{-1}$  is assumed.

Specification	Timepix3	VeloPix
pixel dimension	$55 \times 55 \mu\text{m}^2$	$55 \times 55 \mu\text{m}^2$
matrix size	$256 \times 256$	$256 \times 256$
timewalk	$< 25 \text{ ns}$	$< 25 \text{ ns}$
Time over Threshold range	10 bit	6 bit (calibration mode only)
leakage current compensation (per pixel)	20 nA	20 nA
Time stamp resolution	1.6 ns	25 ns
Time stamp range	18 bit	9 bit
average pixel hit rate	n.a.	600 MHits/s
peak pixel hit rate	80 MHit/s	900 MHits/s
peak super-pixel packet rate	n.a.	520 MHits/s
min. output bandwidth	2.56 Gbit/s	18 Gbit/s
max. pixel hit loss at max. rate	-	1%
power consumption per ASIC	$< 2 \text{ W}$	$< 3 \text{ W}$
radiation hardness	no spec.	$> 400 \text{ Mrad}$
single event upset robust	no	yes

3564 LHC bunch slots are filled, and this corresponds to an average number of interactions  $\nu = 7.6$  per bunch crossing. The assumption for the ASIC is, however, that each bunch crossing will be filled, and hence it should be able to handle a sustained peak rate which is almost a factor 1.5 higher than the average. This worst case approach is chosen because the amount of buffering in the ASIC is not sufficient to fully smoothen rate fluctuations due to the LHC filling scheme. An average number of 8.5 tracks per bunch crossing, as shown in Fig. 50, gives rise to an average (peak) pixel hit rate of about 600 (900) Million per second. Due the packing of hits in super-pixel packets the number of packets is smaller than the number of pixel hits, and amounts to 520 Million (peak) per second.

The timewalk must be less than 25 ns to assure that pixel hits are assigned to the correct bunch crossing. More details are given below.

The total power budget of the ASIC is 3 W, of which about 30% is used by the analog front-end, another 30% by the digital logic, and the remaining 40% is reserved for the high speed serialisers.

The maximum radiation induced leakage current per pixel is calculated to be 7 nA for an operational temperature of  $-25^\circ$  (Sect. 2 ) and hence a safe range of 20 nA for the compensation is specified.

ASICs designed in this 130 nm technology have been shown to be fully operational after a radiation dose of 400 Mrad [19]. Note that only a small fraction of the pixel matrix

faces this harsh radiation environment and that the periphery of the ASIC, which contains analog blocks such as DACs, Phase Locked Loops (PLL) and high speed serialisers will receive a total ionising dose of less than 50 Mrad. Nonetheless the radiation hardness, and especially the non homogeneity across the ASIC will be verified for the Timepix3, and for each version of the VeloPix. The VeloPix, contrary to Timepix3, must be robust against single event upsets. The use of triple-redundant cells is foreseen for configuration registers, memory pointer and counters.

## 6.3 Architecture

### 6.3.1 Global architecture

A block diagram of the architecture of the VeloPix ASIC is shown in Fig. 51. The VeloPix consists of a matrix of  $256 \times 256$  pixels. The data from these pixels is gathered column wise in the End-of-Column (EoC) logic. The column readout direction always points away from the beam, in order to equalize the rate in different columns. The readout direction is indicated by arrows in Fig. 50. Data from the EoC blocks are routed to the 4 output serialisers, each running at a speed of about 5 Gbit/s. The EoC logic and serialisers are located at one side of the ASIC together with all common (peripheral) circuits such as DACs, slow and fast control interfaces. This results in an inactive area of 2-3 mm. The VeloPix operates at a system clock frequency equal to the LHC frequency of 40 MHz, and this sets the resolution for the timestamp. Higher internal frequencies are generated with an on-chip PLL circuit.

### 6.3.2 Front-end analog and digital

The charge sensitive amplifier of the VeloPix basically uses the Krummenacher scheme [20] which gives a constant current discharge while at the same time compensating for sensor leakage currents. This circuit is successfully applied in all generations of Medipix and Timepix ASICs and gives a low noise at the input capacitances typical of planar silicon sensors. For the VeloPix the actual implementation uses an inverted configuration because in this way the leakage current that can be compensated is not limited by the discharge current for electron collecting sensors. The hottest pixel will see a hit rate of about 40 kHz. In order to keep the pile-up up to an acceptable level (1%) the discharge time and hence dead time of the front-end should be below 200 ns. Because of the high-speed discharge, the noise of the VeloPix is higher than that of Timepix3, and is calculated to be about 130 electrons RMS for planar silicon sensors (assuming a capacitance of 50 fF per pixel). This is compatible with an envisaged operational threshold of 1000 electrons. Note that the current generation of Timepix detectors are routinely operated at a threshold of 1000 electrons [21].

Each analog front-end has a high speed discriminator with a common chip-wide threshold and a 4 bit trim DAC to compensate the channel-to-channel threshold offsets. Investigations of the analog front-end are ongoing to check whether it is possible to implement a fast discharge once the signal is over threshold. This option could reduce the dead time of the

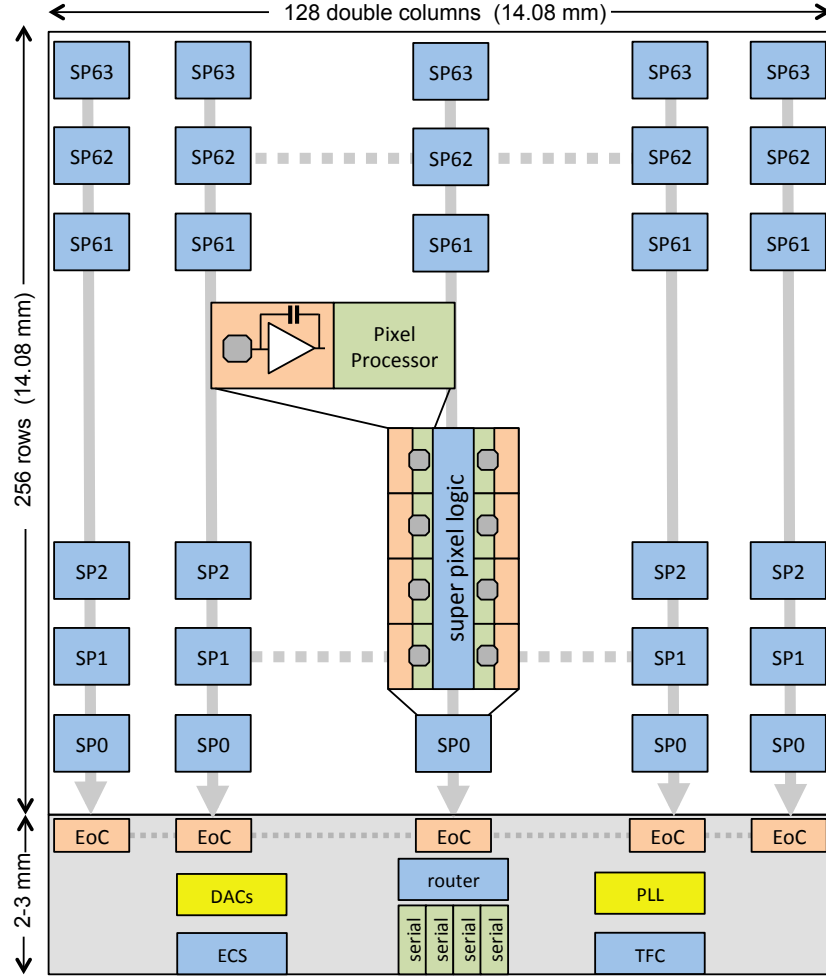


Figure 51: Block diagram of the VeloPix ASIC. Groups of 8 pixels are combined in super-pixels, which are the basic readout units.

pixel to less than 200 ns even for large signals. Signals close to threshold will suffer from time-walk and risk being tagged with the wrong timestamp. Therefore, the pixel features a digital threshold in addition to the (analog) comparator threshold. This digital threshold removes hits which have a small charge and hence large timewalk, and thereby assures that each hit is assigned to the correct bunch crossing. The use of a second threshold raises the effective threshold by several hundred electrons. This is not expected to have a large impact on the efficiency and minimises the contamination of data with out-of-time hits.

Although the pixels are read out in binary mode, the front-end is capable of performing a charge measurement via a constant discharge current and Time over Threshold (ToT) counting. This feature is useful for calibration and monitoring of the detectors, but the readout of ToT information is only foreseen for at a low rate via the slow control interface.

### 6.3.3 Super-pixel concept

Because of the small pixel size and the non-zero track angle, 55% of the tracks will yield a cluster with a size larger than one pixel. Hence quite often two or more adjacent pixels will be hit in the same bunch crossing. Transforming each pixel hit into a separate pixel packet would result in an unnecessarily large amount of redundant data from the timestamp and a large common fraction of the pixel address. Hence it seems beneficial to group together hits in neighbouring pixels for the same bunch crossing. This is achieved by grouping pixels into so-called super-pixels, consisting of a group of  $2 \times 4$  pixels. To minimize the complexity of the super-pixels, and to avoid digital signals crossing the analog region of the pixels, the boundaries of these super-pixels are fixed geometrically. The reduction in bandwidth when sending super-pixel packets compared to individual pixel packets is about 30%. An additional advantage of the super-pixel is that some of the digital functionality in the pixels can be shared which saves area in the layout. Moreover, by placing the digital logic in the centre of the super-pixel the routing is minimized which also leads to a more compact layout.

When one (or more) of the pixels in a super-pixel has a hit, a 9-bit timestamp, corresponding to the LHC bunch crossing number is stored. Each super-pixel has the capability to temporarily store hits from two different bunch crossings in order to minimize the loss of data due to dead time caused by the double column readout of the super-pixels. Readout of the 64 super-pixels in a (double) column is done by shifting down the data from the top of the column to the EoC block via an 23-bit bus running at an effective frequency of 13.3 MHz. Each stage in the double column bus has a buffer in addition to those in the super-pixels. The advantages of this configuration are the short interconnects between the super-pixel and that bus arbitration is done locally. A small drawback is however that the time a packet needs to travel down the column is proportional to the original position of the packet in the matrix. Simulations have shown that the 9-bit timestamp is more than sufficient to unambiguously time-tag hits over this latency. The available bandwidth per (double) column is 13.3 Mpackets/s.

### 6.3.4 End of column logic

At the EoC logic, the column number is added to the super-pixel address. This increases the size of the super-pixel packet to 30 bits as shown in Fig. 52. Four of these super-pixel packets are stored in 128 bit frames<sup>4</sup>, together with an 8 bit header which is used for synchronisation of the frames in the receivers of the TELL40. The data packets collected by the EoC blocks are transported to the high speed serialisers via 8 token controlled busses with a width of 30 bits, each running at a speed of 160 MHz. Each half of the ASIC has 4 data busses where a single bus connects to every 4th EoC block as shown in Fig. 53. In this way the packet rate on these data busses is equalised. The integrated bandwidth of the data busses is 38.4 Gbit/s, which is a factor 2 higher than the available

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<sup>4</sup>Note that the 128 bit frame format assumes the use of the GWT serialiser (see Sect. 6.3.5). When using the GBTx serialiser the format must be adapted to match a 120 bit frame.

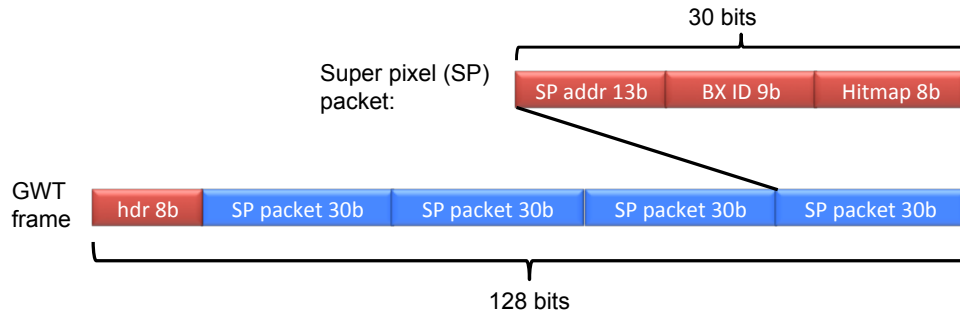


Figure 52: Organisation of data fields in a super-pixel packet, and packing of 4 of these packets in a data frame of the GWT serialiser.

output bandwidth. Note that a fair overhead in bandwidth is required to avoid loss of data due to buffers overflowing. The router between EoC busses and the high speed serialisers

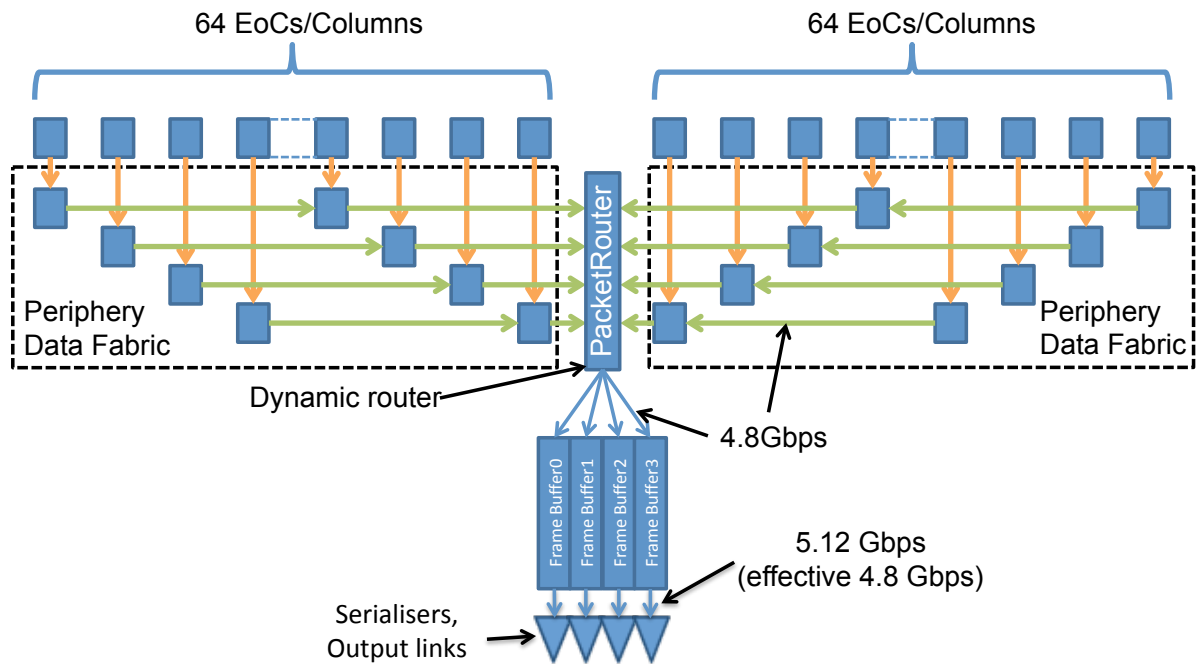


Figure 53: Bus structure connecting the End of Column regions to the high speed serialisers.

distributes the pixel packets over the serialisers. This router is configurable such that all EoC busses can be routed to each serialiser. This allows disabling of serialisers for those ASICs where only a fraction of the bandwidth is required, see Sect. 7.3 for more details.

### 6.3.5 Fast serialisers

For the output serialisers two options are being considered, the GigaBit Transceiver (GBT) and the GigaBit Wireline Transmitter (GWT).

#### **Gigabit Transceiver**

One of the options is to integrate the serialiser and PLL adapted from the GigaBit Transceivers [22]. A group of 4 GBT serialisers, configured in the so-called wide-bus mode yields a total effective bandwidth of 17.92 Gbit/s. Integration of the GBT serialiser onto the VeloPix die requires modifications to the layout because the GBT used a different layer stack than VeloPix (which uses the Medipix3/Timepix3 metal stack). Although these modifications are feasible, they require significant effort because of the high frequencies involved. The main drawback of the GBT serialiser is its relatively high power consumption which is a consequence of its design for SEU immunity. The power consumption amounts to about 300 mW for the PLL and one serialiser. Raising the output bandwidth by increasing the number of GBT units is not advisable given the available power budget.

#### **Gigabit Wireline Transmitter**

The alternative solution for the high speed serialisers, called Gigabit Wireline Transmitter (GWT), will have a power consumption of less than 100 mW for an effective bandwidth of 4.8 Gbit/s. Using four of these serialisers gives a total effective bandwidth of 19.2 Gbit/s which is slightly more than the GBT option. The GWT uses a multi (16) phase Delay Locked Loop instead of a high speed Phase Locked Loop. In this design most of the circuit will run at a speed of only 320 Mbyte/s which is very beneficial for the power consumption. Although the GWT is based on an ePLL development [23] from the CERN electronics group, the design must be improved to overcome the intrinsic limitations due to circuit mismatches which give a severe reduction of the quality of the eye-diagram and hence an increased transmission error rate. A prototype ASIC will be submitted in February 2014 (see also Sect. 7.9) and first results are expected by May 2014. If the GWT performs as expected, the VeloPix will integrate the GWT, and otherwise the GBT will be used.

### 6.3.6 TFC and ECS interface

The VeloPix has to comply with the front-end specifications defined for LHCb [24] [25].

#### **Experiment control system**

For the slow control (ECS) interface, the VeloPix uses two GBTx e-ports [22]. The protocol is a simple serial protocol which is largely (but not fully) compatible with the SPI protocol. Every register in the VeloPix can be read back via the ECS interface. The total number of configuration bits for a single ASIC amounts to about 300k, and all configuration data are stored in SEU robust registers which feature auto-correction in case of a bit flip.

### Timing and fast control

The VeloPix will also be compatible with the basic timing and fast control (TFC) requirements as outlined in [26]. It will respond to the following TFC signals.

- Front-end reset: Assertion of this signal will clear all data from all buffers in the VeloPix but will not reset the configuration settings. To minimize the power surge, the reset will be applied in stages and hence requires up to 64 clock cycles.
- Bunch count reset: When this signal is active, the VeloPix will check and preload its internal 12-bit BCID counter with a configurable offset value. If the BCID counter is not equal to the offset, an error counter is incremented. The lowest 9 bits of the BCID are sent with each pixel packet.
- Sync: When the sync command is given, the VeloPix will send a predefined (configurable) pattern on its serialisers. This is required to synchronise the front-end with the DAQ system.
- Snapshot: Whenever a snapshot signal is given, the ASIC instantaneously captures the value of essential internal counters. These captured values can subsequently be read out via the slow control interface. The snapshot signal allows to check for synchronosity of all front-end ASICs in the system.
- Calibration: The calibration allows the injection of a test signal into the front-end of each pixel at a defined moment in time.

Note that due to the architecture, it is not possible to read out the ASIC in non zero-suppressed mode.

## 6.4 Design and simulation

During the design process many of the building blocks are simulated at various levels of detail. For the analog front-end these are typically transistor level simulations, including the extracted parasitic components from the actual layout of the circuit. To test the performance of the readout architecture, simulations at a high abstraction level have been performed because transistor or even gate level simulations would take too much time for these explorative studies. Hence the architecture is simulated using System Verilog (SV) [27] and uses data from the MC simulations as input. However, when comparing the cluster-size of nuclear interactions in the MC simulation with testbeam data of the Timepix, a large discrepancy in cluster-size was observed. The testbeam cluster-size is substantially bigger, and therefore the MC data has been artificially enhanced in the electronics simulations by adding clusters with a size of 3000 pixels at a rate of 220 kHz. The rate is a factor 1.5 larger than expected (and observed) from nuclear interactions, and also the typical size of a nuclear interaction gives a cluster much smaller than the assumed 3000 pixels. By adding these cluster we test the robustness of the architecture against events with many hits.



The three possible causes for a loss of hits and hence loss of efficiency are pile-up in the pixel front-end, overflow of buffers in the readout architecture and ambiguity of the time stamp due to latency exceeding the 9-bit range of the BCID. Figure 54 shows the loss of efficiency due to the dead time of the pixel front-end assuming the pixel is busy for 200 ns when a hit is received. The loss of hits amounts to 1.5% for the region close to the beam. Note that this loss is for a sustained peak rate of 1.5 times the average rate, and is therefore not the limiting factor for running at high instantaneous luminosity. The right-hand side of Fig. 54 shows that the loss of efficiency due to limitations of the readout architecture is negligible up to the maximum specified rate. However, when increasing the hit (peak) rate by more than 20% beyond the maximum specification of 520 MHz, a rapid increase of the inefficiency and dead time occurs, which is attributed to the limited on-chip bandwidth. This assumes a pessimistic bunch filling scheme, as outlined in Sect. 6.2.

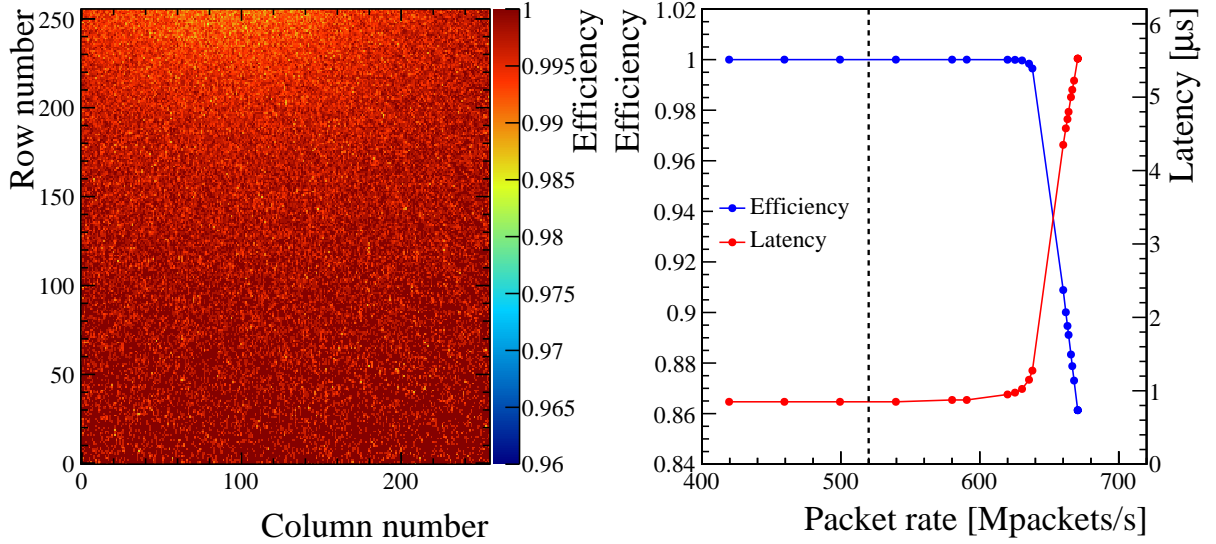


Figure 54: (left) Efficiency of the front-end. The loss is due to dead time. A fixed dead time of 200 ns per hit is assumed. (right) Efficiency of the digital readout architecture. The dashed line indicates the operating point obtained from the MC simulation, without the injection of high occupancy events.

The analog part of the pixel cell is designed as a full custom layout, as are the PLL and the high speed sections of the output serialisers. The digital logic in the matrix is synthesized using a High Density (HD) cell library. This HD library was developed for, and successfully applied in, the Medipix3 and Timepix3 ASICs and gives more than a factor two reduction in the area per cell compared to the standard cell library of the technology design kit. For the EoC logic where the area is not critical, the faster standard cell library is used because these blocks run at a higher clock frequency.

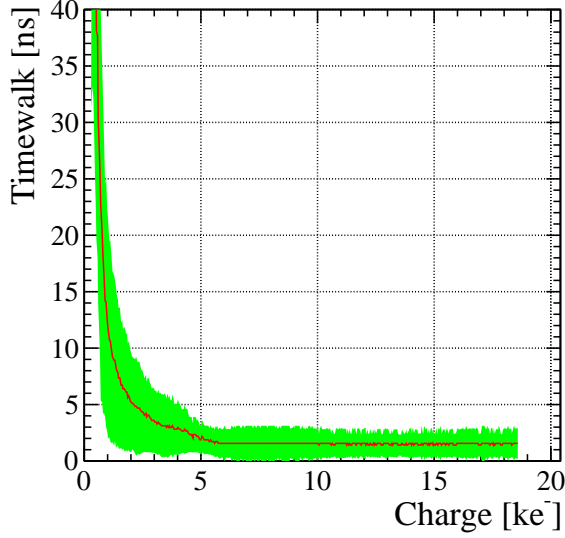


Figure 55: First timewalk measurement for a single pixel of the Timepix3 using a 500  $e^-$  threshold. The plot shows that the timewalk is less than 25 ns for charge injections larger than 1  $ke^-$ .

## 6.5 Prototyping

The Timepix3 ASIC is the basis for the development of the VeloPix ASIC, and can be considered a lower speed version of our final ASIC. Because of the large commonality between the ASICs, manpower from the VeloPix project has been assigned to the Timepix3 development in order to speed up the process, and thereby have a radiation hard prototype ASIC in hand as soon as possible. At the same time we profit from the available knowledge to make full scale pixel ASICs. The Timepix3 ASIC has recently been received back from the foundry and testing of the ASIC has started. Thus far the ASIC works as expected and the results show very good agreement with the simulations. The data-push architecture seems to work properly, but the proper testing of the ASIC in terms of synchronosity and efficiency requires beamtests. One of the major changes from Timepix to Timepix3 is a large increase of the front-end speed which drastically reduces the timewalk. Figure 55 shows a first timewalk measurement of the Timepix3 for a single pixel, using testpulses and a threshold of 500 electrons (no sensor attached). The timewalk is less than 25 ns for signals as low as 1  $ke^-$ , but can be larger than 25 ns for signals very close to the threshold. Application of a second digital threshold as described above will remove these low charge hits and assure that all remaining hits are assigned to the right bunch crossing.

The design of the VeloPix is ongoing at full speed and submission of the first full scale ASIC is aimed for by Q3 2014. However it is clear that there will be no tested ASIC available before the end of 2014 and hence our sensor irradiation programme as described in Sect. 5.2 will be carried out using the Timepix3.

Before the VeloPix ASIC will be submitted there are several issues that must be proven. One of them is the robustness against Single Event Upsets. Although the technology used for Medipix3 and Timepix3 is tolerant to ionising radiation, these ASICs are not robust against SEUs. To achieve this, the static configuration parameters will be stored in triple redundant registers. Depending on the SEU sensitivity of the cells in the new HD library,

some dynamic structures like FIFO pointers might also need to be triplicated. To test the SEU sensitivity of the flip-flops an irradiation with heavy ions will be carried out at the Heavy Ion Facility in Louvain la Neuve with a Medipix3 ASIC. The irradiation is planned for December 2013. Another part of the project which is considered too risky to directly integrate into the full scale ASIC is the GWT serialiser. Hence a  $2 \times 1$  mm prototype ASIC with this serialiser and the PLL circuit providing the reference clock will be submitted in February 2014. This testchip also contains various on-chip (pseudo random) pattern generators to feed the serialiser. These pattern generators are triple-redundant to allow testing of the SEU sensitivity of the GWT. In addition to the sensor irradiation programme testbeams will also be used to check the response and synchronosity of the ASICs using beams of charged particles. For 2014 the focus is on testing the Timepix3 with prototype VELO pixel sensors. A low rate beamtest is planned for February 2014 at the DESY testbeam facility using a 5 GeV electron beam. Later in 2014 a high rate beam test is foreseen at the high rate test facility in Fermilab. Beam testing of the VeloPix will take place early 2015 in the testbeam area at CERN.

## 7 Electronics

### 7.1 System Architecture

As is the case for the current VELO electronics, the system consists of as many parallel replicas of identical electronic chains as the number of modules. A chain is shown in Fig. 56. The decision not to have any optical component (lasers, diodes, fibres and optical connectors) inside the secondary vacuum has a profound impact on the architecture. This decision is motivated by the difficulty of cooling the high-power dissipating optical components in vacuum, their sensitivity to radiation, the delicateness of the interconnections, the additional mass in the detector acceptance and the nearly impossible access for maintenance and repair during operation. As a consequence, many high speed signals for control and data readout must be routed on low mass electrical cables from the modules through the vacuum wall to the electro-optical transition boards located on the periphery of the vacuum tank. For similar reasons, the decision was taken to locate all DC/DC converters powering the front-end ASICs in an accessible area outside the vacuum tank. These two functions of electro-optical transition and DC/DC powering are combined on a single board called Opto and Power Board “OPB”, described in Sect. 7.4. An additional benefit of this approach is that it significantly reduces the radiation doses received by many electronic components in the system. We benefit enormously from the fact that many of the front-end electronic components in the system, with the notable exception of the VeloPix ASIC, have been developed by the “versatile link” project [28] and the “radiation hard DC/DC converter” project [29]. These components are radiation qualified to higher fluences than required in our application. All optic fibres to and from the OPBs are routed to the TELL40 and SOL40 [25] systems in the surface building. These fibres and the TELL40 boards are commonly developed and installed by the LHCb collaboration. The VHDL firmware running on the TELL40 specific to processing the VELO data packets are developed by the VELO group and discussed in Sect 8.1. All above points are detailed in following sections.

### 7.2 Front-end hybrids

The integration and prototyping of the front end hybrid are discussed in Sect. 5.4. This section covers the electrical functionality of the hybrid.

#### 7.2.1 Construction

The total power supply requirement of each tile ( $\geq 5$  A at 1.5 V) and very high frequency operation  $\geq 5$  GHz, demands a low resistance and low impedance power distribution layout, achieved by two 15  $\mu\text{m}$  copper planes separated by a 50  $\mu\text{m}$  dielectric layer. The upper of these two planes is a complete ground plane, whilst the lower inner layer will provide segmented power distribution for analog and digital supplies. Furthermore two 15  $\mu\text{m}$  copper layers are needed for signal and high voltage routing and are applied on either side of the central power distribution layer pair. The top layer, and parasitically the bottom

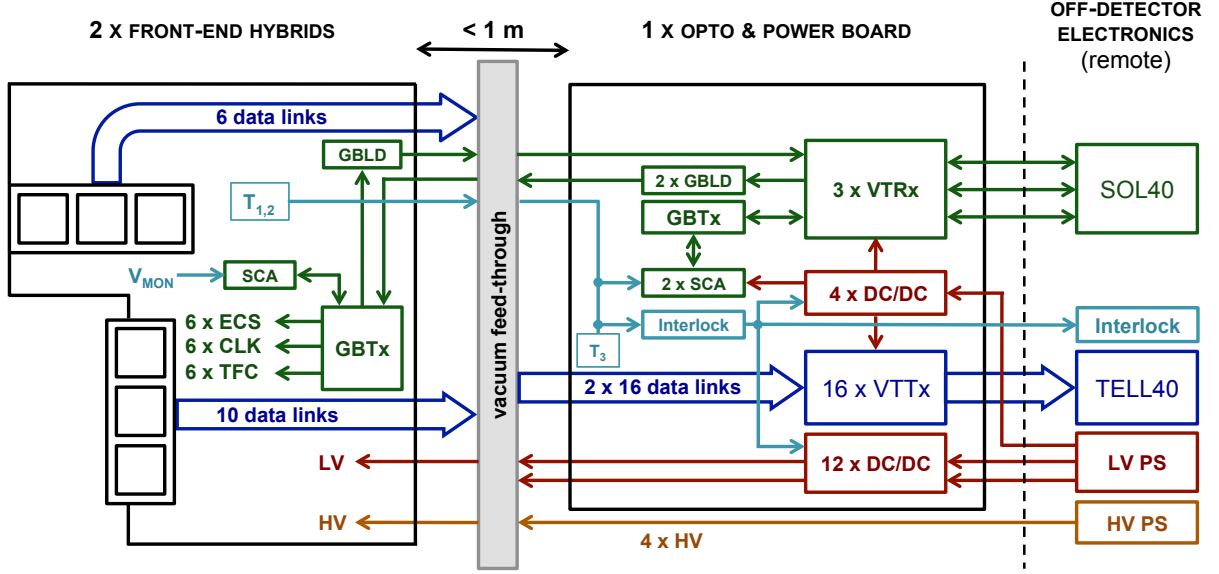


Figure 56: Schematic picture of the VELO electronics. Each opto and power board will serve the two front-end hybrids located at opposite sides of one detector module. The two hybrids are electrically identical but geometrically different due to the asymmetric shape of the module. The granularity of the off-detector electronics is not correctly represented in the figure.

layer, are plated with  $3\text{ }\mu\text{m}$  nickel and a sub-micron layer of gold for wire bonding. The

Table 10: Summary of the number of items needed in terms of links, power supply channels and key electronic components. Numbers are given both per detector module and for the full VELO system, assuming 52 detector modules.

Item	per module	VELO total
Data links	32	1664
Control links	3	156
VTTx units	16	832
VTRx units	3	156
VeloPix	12	624
GBTx	3	156
SCA	3	156
GBLD	4	208
DC/DC modules	16	832
LV channels	3	156
HV channels	4	208

40 MHz clock and control lines are routed on the top and bottom layers, however the very high frequency differential output signals from the VeloPix chip require that the trace lengths, trace separation, dielectric type, thickness and uniformity are tightly controlled to ensure signal integrity. Hence these signals are confined to the top layer of the circuit above the continuous ground plane and the routing distance to the connector is minimised. Another consideration for these fast signals are high frequency dielectric losses which degrade signal rise time when these signals are to be driven over the 70 cm length of cable, described in Sect. 7.3. To ensure a good impedance match between the cable and the hybrid, the top layer dielectric of the circuit and that of the cable are made of the same thickness and material type. A single 20  $\mu\text{m}$  solder resist is applied to the top surface and to the underside to provide electrical isolation from the silicon cooling substrate. The total thickness of the circuit is therefore  $20 + 15 + 50 + 15 + 50 + 15 + 50 + 15 + 20 = 250 \mu\text{m}$ . If a thicker top dielectric of 100  $\mu\text{m}$  is required, it will increase to 300  $\mu\text{m}$ . Assuming a 50  $\mu\text{m}$  adhesive layer for attachment then the total height of the bond pads above the substrate is 350  $\mu\text{m}$ . If possible, conservative industry-standard design rules of 100  $\mu\text{m}$  track and gap with 300  $\mu\text{m}$  plated through holes will be used allowing for possible manufacture by multiple vendors.

### 7.2.2 Electrical functionality

The front-end hybrid has a common ground plane for the two pixel tiles and distributes four separate analogue and digital supply voltages for the two tiles. The GBTx, SCA and GBLD are powered from separate supplies as described in Sect 7.4. The two high voltage bias lines are filtered separately and the pixel positive polarity of the supply is tied to hybrid ground in a single point. The two pixel tiles are then biased separately by these supplies.

The GBTx ASIC receives the clock and control signals from the OPB and decodes these for distribution to the VeloPix ASICs. Six clock outputs are used to distribute the 40 MHz clock point-to-point to the six VeloPix ASICs. The TFC and configuration commands are also transmitted individually to each VeloPix using the e-links provided by the GBTx ASIC. They are also used to read back configuration and monitoring data from the VeloPix ASICs. The supply voltages and DAC output voltages are monitored via the SCA ASIC mounted on the front-end hybrid.

The monitored data is transmitted back to the OPB via the GBTx ASIC, using an additional GBLD with pre-emphasis to drive the signals over the high speed cables. The hybrid temperature is monitored by the OPB to allow temperature monitoring also when the hybrid is not powered.

## 7.3 Electrical high speed cables

Several high speed signals must be routed between the peripheral OPB boards and the modules. Since the cables carrying these signals have to be fed through the vacuum wall, they consist of a short cable segment (50 to 75 cm) inside the vacuum tank and a short

vacuum feedthrough segment ( $\sim 10$  cm). The number of signals, the construction of the cable, the signal integrity, the connectors and the two segments are detailed below.

### 7.3.1 Number of signals

The four VeloPix ASICs that are surrounding the beam hole see the highest track rates and will require all four serial output links to transfer the data. The other eight ASICs that are further away from the beam need only two or one links. To avoid a complete loss of a VeloPix ASIC in case of a failing link, we use a minimum of two links per ASIC. Thus the detector tiles closest to the beam will have  $4 + 4 + 2 = 10$  data readout links, whereas the outermost tiles will have only have six. Each side of the module thus has 16 data readout links. The total number of data links assuming 52 detector modules is 1664. The GBTx on either side of the module will also have two high speed signals each, one in each direction.

### 7.3.2 Cable construction

All these signals have data rates close to 5 Gbit/s and are differential signal pairs with CML (current mode logic) electrical levels. To minimise EMI, the cables are implemented as edge-coupled strip lines, with characteristic impedance close to  $100\ \Omega$  and intermediate grounded guard traces between the pairs to reduce crosstalk, as shown in Fig. 57. The signal and ground traces will be spaced by 0.4 mm, equal to the pitch of the pins on the MOLEX connectors. The trace widths are  $240\ \mu\text{m}$  and the gaps are  $160\ \mu\text{m}$ . The width occupied by a signal pair with guard traces on either side is thus  $3 \times 0.4\ \text{mm} = 1.2\ \text{mm}$ . Hence the widths required for the readout lines of the innermost and outermost tiles are therefore 12 mm and 7.2 mm, respectively. Prototypes have been constructed with a special laminate (Pyrallux AP-plus) from Dupont that is targeted for these types of high speed signal transmission applications. Its main features are a dielectric with a tightly controlled thickness available up to  $300\ \mu\text{m}$  and with copper layers with special surface finish<sup>5</sup> to minimise the skin effect. A cable with a total dielectric thickness of  $350\ \mu\text{m}$  is optimal, see Sect. 7.3.3. The resulting total cable thickness, including  $2 \times 36\ \mu\text{m}$  external copper planes and  $2 \times 20\ \mu\text{m}$  cover lay is approximately  $460\ \mu\text{m}$ .

### 7.3.3 Signal integrity

At data rates of 5 Gbit/s, great care must be taken to minimise signal distortion. Most importantly, the transmission length must be minimised, but depending on the details of the mechanical design of the vacuum tank, this length is between 50 and 75 cm. Up to data rates of 8 Gbit/s, the contribution to signal distortion due to the skin effect of the conductors is still dominating over the contribution due to the loss of the dielectric. The loss factor is  $D_f = 0.002$  at 10 GHz for Pyrallux AP-plus. Therefore, the trace width should be as large as possible. But the width is related to the dielectric thickness  $H$ , since

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<sup>5</sup>The surface has a very low  $R_a$  roughness, defined as the arithmetic average of the roughness profile.

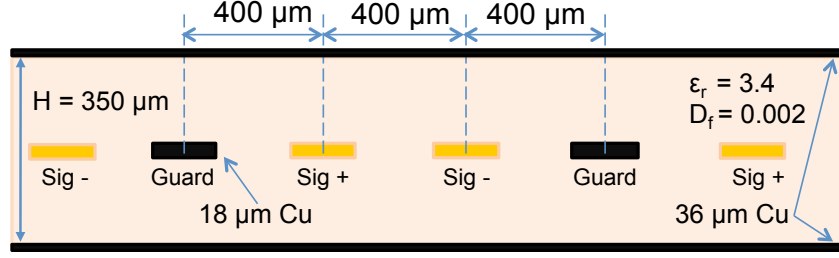


Figure 57: Figure showing the strip-line layout of the high speed electrical cables. The trace widths are  $240\ \mu\text{m}$  and the spacing is  $160\ \mu\text{m}$ .

a  $W/H$  aspect ratio of approximately 0.6 is required to obtain a differential transmission line impedance of  $\sim 100\ \Omega$ . On the other hand the thickness of the dielectric should be limited, since these cables have to be flexible enough to absorb the motion during the opening and closing of the detector halves ( $\sim 3\ \text{cm}$ ). Therefore a compromise between flexibility and signal distortion must be found for the dielectric thickness. Prototypes with  $500\ \mu\text{m}$  and  $350\ \mu\text{m}$  have been produced and tested (see Sect. 7.9) and the latter fulfills both requirements of signal integrity and flexibility. To further enhance signal integrity of the data links, the GWT serialiser & driver of the VeloPix features a pre-emphasis circuit tuned to the characteristics of these cables. All segments of these cables and part of the OPB board should use the same material and construction to preserve the same characteristic impedance.

### 7.3.4 Connectors

The various interconnections between hybrid circuits, readout cables, vacuum wall feedthroughs and OPB boards will use the MOLEX Slimstack  $0.4\ \text{mm}$  pitch board-to-board connectors. These miniature connectors are found to induce very low insertion loss ( $0.1\ \text{db}$ ) at GHz frequencies. The housing material is LCP and radiation hard beyond  $1\ \text{GRad}$  [30].

These are very low mass and are available with up to 80 pins with a mated height of just  $1\ \text{mm}$  and stated current capability of  $300\ \text{mA}$  per pin.

### 7.3.5 Vacuum feedthroughs

A short length flexible cable with the same build as the data cables will be passing through a slit in the metal wall of the vacuum tank. It will have connectors on both ends to connect to the data readout cables to the OPBs. These will be preinstalled and tested before the OPB and modules are installed. Details of the construction and mechanical integration are given in Sect. 10.2.3. Separate feedthroughs will be used for the LV and HV cables.



## 7.4 Opto and power board

The VELO opto and power boards (OPB) are located immediately outside of the secondary vacuum enclosure, in a crate mounted directly on the vacuum tank. It supplies voltages and sends and receives signals through the vacuum feedthroughs and electrical cables described in Sect. 7.3. One board will serve the two front-end hybrids located at opposite sides of one VELO detector module. A schematic view of the functionality is shown in Fig. 56. The OPBs have the following functionality, that will be described in the following paragraphs:

- It performs the electrical to optical conversion of the serial data links;
- It performs the electro-optical conversion of the control and monitoring signals and transmits them to the front-end hybrid;
- It performs the DC/DC conversion of the supply voltages and distributes them to the front-end hybrid and locally on the board;
- It monitors the voltages and temperatures of the front-end hybrid and the OPB and issues an interlock signal in case of an over-temperature.

Each hybrid has six VeloPix ASICs that generate 16 high-speed serial data streams in total. Hence each OPB has to provide electrical to optical conversion for 32 serial links. This is done by 16 VTTx units [28] mounted on the board. These units provide two laser drivers (GBLD [31]), two laser diodes and an edge fibre connector. The board provides a minimum distortion signal path from the vacuum feedthrough to the VTTx units.

The OPB has three bi-directional control links where the opto-electrical conversion is performed by three VTRx [28] units. They have a diode to receive control signals and a laser driver and diode to return monitoring data, and an edge fibre connector. Two of the control links are routed directly to the two front-end hybrids where they are decoded by the GBTx chip [22]. The signals are driven through the high-speed cables by GBLD ASICs mounted on the OPBs and on the front-end hybrid. These GBLD ASICs have a tuneable pre-emphasis to compensate for the signal distortion on those cables. The third control link is decoded by a GBTx chip located on the OPB and handles the control and monitoring of the board itself via two SCA chips. It is the slow control ASIC in the GBT family and provides the I<sup>2</sup>C buses required to configure the laser drivers and the digital signals needed to control and monitor the DC/DC converters.

The OPB receives three supply voltages from the LV power supplies, as described in Sect. 7.5. Two of the voltages are used to supply the two front-end hybrids. Each pixel tile, comprising of three VeloPix ASICs, receives one analogue and one digital voltage provided by two DC/DC converter. Each one is implemented on a small mezzanine board [29]. Hence in total eight DC/DC converters are needed to supply the VeloPix ASICs on the two hybrids. Four additional DC/DC converters are used to supply the GBTx, SCA and GBLD ASICs on the two hybrids. The third supply voltage is fed to four DC/DC converters that provide the two voltages needed for the OPB itself.

Table 11: Power dissipation estimates for the OPB and detector module.  $V_{\text{IN}}$  and  $I_{\text{IN}}$  are the input voltage and current to the device.  $P_{\text{HYBRID}}$  and  $P_{\text{OPB}}$  are the heat dissipated in the hybrid and OPB, and  $P_{\text{PS}}$  is the power delivered by the power supply. The difference is the heat dissipated in the 60 m supply cables. The first three lines in the table correspond to the three power supply channels.

Device	$V_{\text{IN}}$ [V]	$I_{\text{IN}}$ [A]	$P_{\text{HYBRID}}$ [W]	$P_{\text{OPB}}$ [W]	$P_{\text{PS}}$ [W]
OPB	5	5	0	25	37
Hybrid (front)	1.5	11	16.5	5.5	31.5
Hybrid (back)	1.5	11	16.5	5.5	31.5
Total (module)			33	36	100
Total (VELO)			1700	1900	5200

The DC/DC converters supplying the voltages for the hybrid, the VTTx for the data links and the two VTRx for the hybrid control can be enable and disabled remotely via the SCA ASIC. However, the DC/DC converters supplying the voltages for the local control of the OPB are always enabled. The voltages at the input and output of the DC/DC converters are monitored by the SCA ASIC.

The power dissipation estimates are based on the maximum values given in the design specifications of the components on the front-end hybrid and the OPB. The power dissipation estimates are given in Table 11, assuming that the average consumption will be 80% of these values. The total power dissipated in the detector module is 33 W and it is 36 W in OPB. Assuming 52 VELO modules the total power dissipated in the OPBs is 900 W per side, to be compared to the 300 W per side for the current VELO. Hence active cooling is required for the OPBs.

The temperature of the detector module is monitored by two thermistors, labelled  $T_{1,2}$  in Fig. 56. The temperature is measured by the SCA chip [32] and is also monitored by an interlock circuit. The temperature of the OPB itself is monitored in a similar way. The DC/DC converters supplying the hybrid and laser driver voltage are disabled locally in case the temperature goes above threshold. Moreover, an interlock signal is sent off detector to disable the LV and HV supplies as described in Sect. 7.7. The state of the interlocks are monitored by the SCA chips.

## 7.5 Power supplies

The high and low voltage supplies are located in the underground counting rooms behind the shielding wall. The low voltages are brought to the OPB by long-distance copper cables using sense wires to ensure that the correct voltage is supplied to the input of the DC/DC converters. Three voltages are supplied to each OPB (see Sect. 7.4), two for the

two hybrids served by that board and one for the electronics located on the board. The required current on each channel is less than 5 A and the cable resistance is estimated to be approximately  $0.5\ \Omega$ . Hence the required output voltage of the power supply is less than 7.5 V. The total power per supply channel is given in Table 11. The total number of required channels with this specification is given in Table 10.

The high voltage silicon bias is supplied to the front-end hybrid via a separate vacuum feedthrough without passing through the OPB. The voltage is supplied via three lines: HV, HV return and shield. Four floating high voltage channels are provided for each detector module, one for each pixel tile. The maximum voltage provided is 1000 V at a maximal current of 1 mA. The total number of high voltage channels is given in Table 10.

## 7.6 Detector grounding scheme

We adopt a similar grounding scheme to that of the current VELO. All voltage supplies are referenced to a single point which is the ground plane of the front-end hybrid circuit. The hybrid ground is galvanically linked to the potential of the RF box to avoid beam induced pickup. This is achieved by a ground strap connecting the hybrid ground to the detector base on which the RF box is mounted. Ground loops in the power return are avoided by isolating the ground of the OPBs from the metallic support structures. All low and high voltage supplies are floating with the return line referenced to ground on the front-end hybrid.

## 7.7 Interlock system

A temperature interlock signal is generated by the opto and power boards in case the temperature of the detector modules or the OPB exceed predefined limits. These signals are routed back to the underground counting room and received by the VELO interlock box. This also receives signals from the cooling system, vacuum system and LHC beam interface. Enable signals are provided to the high and low voltage supplies when all systems are in the correct operational mode and the temperatures are below the interlock limits.

The state of all the inputs to the interlock box are communicated to the detector control system for monitoring purposes. The decision of the interlock box and the states of its output signals are also monitored by the detector control system.

## 7.8 Radiation qualification

The VELO electronics are located in four areas, on the detector module, on the opto and power boards and in the underground and surface area counting houses. The equipment in the two latter areas are not exposed to any radiation and hence are not discussed further here. The dose levels on the detector module can be estimated from extrapolating the fluence profile shown in Fig. 9 and are summarised in Table 12. The table also gives the

Table 12: Estimated dose levels after  $50 \text{ fb}^{-1}$  for the locations where the VELO electronics components are situated. The second column gives the radial distance from the beam, the third column gives the equivalent NIEL fluence and the fourth column gives the Total Ionising Dose (TID).

Location	$r$ [mm]	$\Phi$ [ $\text{n}_{\text{eq}}/\text{cm}^2$ ]	TID [MRad]
Detector module			
VeloPix (max)	5	$8 \times 10^{15}$	400
GBTx & GBLD	60	$9 \times 10^{13}$	4.5
Opto and power boards	600	$13 \times 10^{12}$	0.23

corresponding total ionising dose<sup>6</sup>.

The estimated radiation levels for the OPBs are also given in the table. These are based on simulations performed for the current detector [33], where the values are scaled up with the increased integrated luminosity and with the larger total cross section currently assumed (102.5 mb, see Table 1) compared to those used for the dose estimates (80 mb). The distance from the interaction point to the closest point of the OBP will be the same as that for the current repeater boards.

The components on the detector modules are either passive components or custom made ASICs in 130 nm CMOS technology designed using radiation tolerant design rules. The GBTx, SCA and GBLD ASICs are qualified by the design teams and the qualification of the VeloPix is described in Sect. 6.

The majority of the components on the OPB are qualified by the designers. In addition to the components that are common with the front-end hybrid, this is also true for the VTTx, VTRx and the DC/DC converters. Hence no further qualification is required for these items. The only remaining item with active components that need radiation qualification is the circuitry for the interlock. It is made of commercial components on a mezzanine board that will be qualified through an irradiation campaign of the fully assembled board.

## 7.9 Prototyping

### 7.9.1 Electrical high speed cable prototypes

Two prototype series of the high speed cables have been produced and tested. The first series was using a  $500 \mu\text{m}$  thick dielectric layer and conductor trace width of  $280 \mu\text{m}$ . The aims were to measure: characteristic impedance, crosstalk between signals, insertion loss of

<sup>6</sup>The radiation is dominated by minimum ionising particles in the area where the front-end hybrids are located and 1 MRad TID is assumed to correspond to a NIEL fluence of  $2 \times 10^{13} \text{ n}_{\text{eq}}/\text{cm}^2$  in silicon.

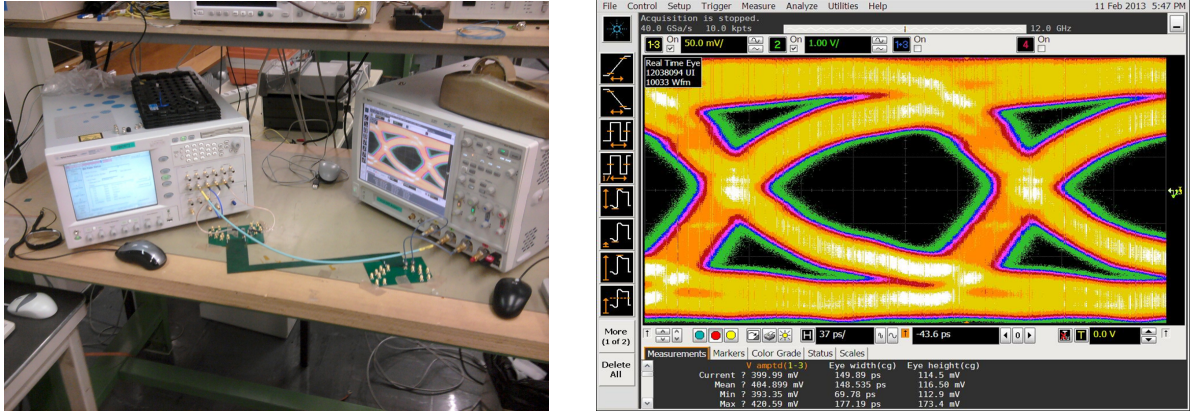


Figure 58: (left) Photograph of the setup used to evaluate the prototype high speed cables. (right) Eye diagram of a signal at the end of the prototype high speed cable.

MOLEX slimstack connectors and S-parameters characterisation as well as eye diagrams. The obtained results were compared to predictions by simulation tools to check their accuracy. In a second version of prototypes, the dielectric layer was reduced to  $350\text{ }\mu\text{m}$  and conductor trace width to  $240\text{ }\mu\text{m}$  on a line-spacing of  $400\text{ }\mu\text{m}$ . With these prototypes, we examined insertion loss due to wire bonding and loss due to intra-pair skew created by a 90 degrees bend of the traces. Fig. 58 shows the measurement setup and an eye diagram of a transmission over 40 cm at 4.8 Gbit/s, including test cables and adapters. New prototypes for the cables and vacuum feedthrough will be built with a shape and size adapted to the final module and OPB design. This will allow studying the end-to-end performance of a transmission link as well as the mechanical flexibility of these cables.

### 7.9.2 OPB prototyping

This board uses extensively components, such as the GBTx, SCA, GBLD, VTTx, VTRx and DC/DC, that will become available in early 2014. Small scale prototypes will be built to study the quality of data transmission over a complete data readout link, *i.e.* including the electrical high speed cable prototypes and vacuum feedthroughs as input and 400 m optical fibres at the output. The GWT prototype serialiser & driver (see Sect. 6.3.5) will be evaluated as a data source and signal driver.

### 7.9.3 DC/DC tests

The influence of the proposed powering scheme on the front-end performance will be investigated using the Timepix3 ASIC. It will be powered with a DC/DC converter with and without an additional linear regulator to compare the noise performance. Moreover, the effect of the short-distance cable between the DC/DC converter and the front-end ASIC will be investigated this way.

## 8 VELO DAQ integration

The upgraded VELO requires an entirely new readout and control system. The proposed electronics architecture is described in [25]. The TELL40 is a common readout board being developed for LHCb [34]. At the time of writing, two variants of the TELL40 are being considered for the data acquisition system (see Fig. 59). The first is similar to the currently installed detector, where dedicated boards with FPGAs sit in a crate and are controlled via a credit card PC interface. The second option would move the FPGAs inside PCs, by placing them on PCIe cards [35]. Although the implementations for each option are quite different, their functions remain the same, and the FPGA is the same. In terms of firmware development and prototyping of a solution for the VELO upgrade, there is no difference. Henceforth, the TELL40 described in [34] is used as the baseline solution and any development work is assumed to apply equally to either readout solution.

For the VELO, specific firmware and software must be developed for the TELL40. This will require scaled prototypes for testing. The VELO would use 20-22 input links to each FPGA utilising an average data rate of 20-30 Gbit/s (with a peak of  $\sim 50$  Gbit/s). This results in a minimum of 78 FPGAs to serve the entire detector. Similar to the TELL40, a common control and monitoring board is also being developed, known as SOL40. For control and monitoring, an additional 6 units operating as SOL40 cards would serve for the whole system. Table 13 shows the estimated requirements for the DAQ, and control of the VELO.

Table 13: Minimum unit requirements for the VELO upgrade DAQ.

DAQ FPGA units	78
Control/Monitoring FPGA units	6
ATCA Motherboards	22
ATCA Crates	2

### 8.1 VELO firmware and software, ECS

The TELL40 requires specific firmware to deal with the data coming from the VeloPix chips. The data arrives out of time, and is already zero-suppressed by the VeloPix ASIC. The chief functions of the firmware are to time-order the data into hits from the same bunch-crossing, and then assemble it such that it can be sent to the event builder farm. Clustering neighbouring hits in the firmware may also be possible. This would be a significant time-saving in terms of CPU processing on the trigger farm. However, clustering in the firmware requires investigation to determine its feasibility.

Firmware components for reception and decoding of the serial data received from the front-end will be provided as common LHCb components on condition that the GBT is used. However, should the VeloPix ASIC use the GWT transceiver a separate decoding

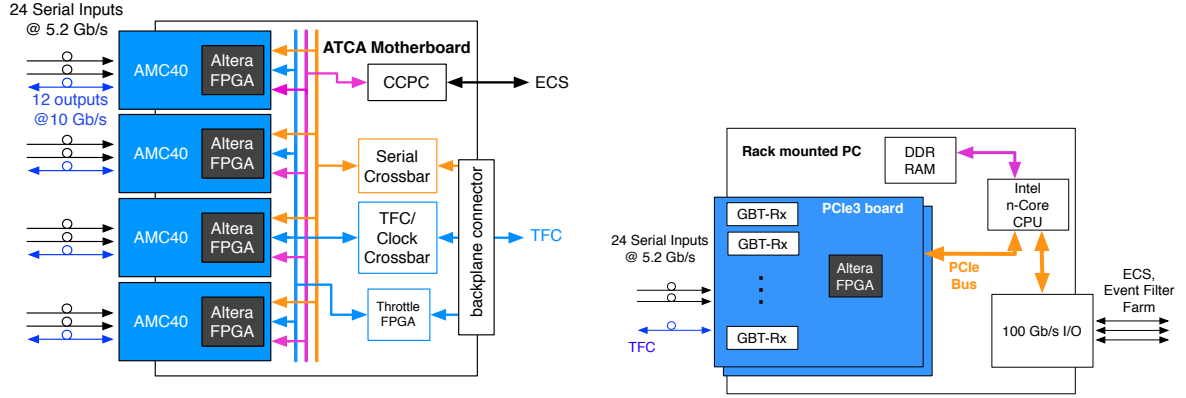


Figure 59: (left) Diagram of a TELL40 ATCA readout board with AMC mezzanines. Inputs and outputs show connections to the VELO modules and the control software. (right) Diagram of a PCIe40 readout system. Each board would contain one high-end Altera FPGA. Data is output over the PCIe3 bus to the CPU which handles gigabit transmission to the event builder farm.

will be needed for the VELO data - see Sect. 6.3.5 for details. The high rate of data coming from the VeloPix chips presents the most significant challenge for the VELO firmware. The data must be processed fast enough such that losses do not occur. Enough buffer space must be made available to deal with large instantaneous bursts of data. A diagram of the planned VELO firmware is given in Fig. 60. FPGA resource utilisation of VELO specific firmware blocks (GWT decoding and time-ordering the data) are under investigation. The GWT decoding is expected to be similar to that of the GBT.

The SOL40 common control and monitor board will be used to send configuration signals to the VeloPix chips, along with TFC information such as the clock, trigger, and front-end reset signals. It will communicate with the OPB, and activate the DC/DC and laser driver power. The SOL40 will also be used to record temperature and voltage information from the OPB and module to the monitoring software. The SOL40 will not require specific VELO firmware. The firmware will be generic for LHCb and will cover all of the necessary communication protocols such as SPI, and I<sup>2</sup>C. The choice of protocol will be determined from definitions in the control software. Creating these definitions and testing them will be the responsibility of the VELO DAQ team.

The control and DAQ software for the VELO upgrade will be developed using the Siemens WinCC framework. This same framework is used for the current LHCb detector. The control software will create a virtual representation of the hardware hierarchy. Several WinCC projects will be developed for each of the VELO subsystems. This includes the VELO modules themselves, HV, LV, TELL40, SOL40, cooling, vacuum, motion and interlock systems. Monitoring must be in place to display live status of the detector, and to record temperatures, voltages and other pertinent information to the LHCb Conditions Database. Alarm systems must be developed to raise alerts and to perform automatic safety actions to protect the detector, and the Detector Safety System (DSS) will be adapted to the needs of the new detector.

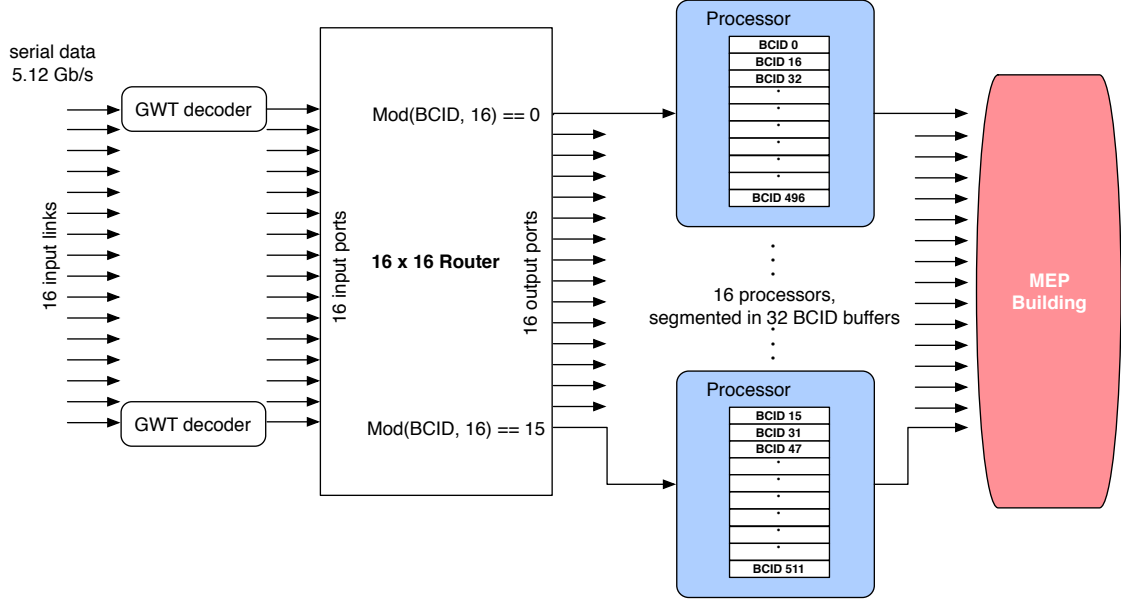


Figure 60: Block diagram of the VELO part of the TELL40 firmware. Super-Pixel Packets (SPP) from the front-end are decoded and passed to a routing network which routes the data by LSBs of the bunch count. The processors accumulate hits from the same event and pass them to the event builder where clustering may be performed. The final events are sent to the gigabit output buffers. Numbers shown assume 16 input links but can be scaled to follow different input specifications.

## 8.2 VELO DAQ slice development

The TELL40 motherboard has four mounted AMC mezzanine cards, both based on the ATCA standard [36]. Each of the four mezzanines receives data from up to 24 opto-links operating at 4.8 Gbit/s (see Sect. 7.4).

The first objective for DAQ testing is to build a TELL40 slice. This will consist of a single AMC card [37] with the final (or close to final) Altera FPGA chip (Stratix V or Arria 10). The slice will run the initial developments of the VELO readout firmware and be primarily used for readout tests of the VeloPix chip and to progress the VELO TELL40 firmware. The VeloPix chip will be used as input to the TELL40 prototype. Another goal is to develop a self-testing mechanism for the slice. Simulation data emulating the output of the VeloPix chip will be generated, either by means of another FPGA or the production FPGA on the AMC mezzanine. This allows independent testing of the FPGA and firmware, and can be used to isolate problems upstream.

A second stage slice will be developed which will essentially evolve to the full TELL40 system. In this second phase, the SOL40 will be added to the system. The TELL40 firmware should be in a workable state, and development and testing of the ECS software can begin.



## 9 Cooling

This section describes the in-vacuum, evaporative CO<sub>2</sub> cooling system for the pixel modules. The current VELO pioneered the use of evaporative CO<sub>2</sub> cooling in high energy physics. The  $\sim 1$  kW power dissipated by the VELO is removed and the sensor tips are kept at around  $-7^\circ\text{C}$ , which is essential to control the leakage current of the silicon sensors after irradiation and prevent degraded performance or even thermal runaway.

At the upgrade, there will be a more challenging radiation environment, and a marked increase in heat load due to the use of the VeloPix ASICs. The cooling remains CO<sub>2</sub> based, however the cooling substrate is integrated directly into the module, in contrast to the current system where the coolant runs in an independent manifold and the connection to the modules is made *in situ*. The cooling substrate forms the mechanical backbone of the VELO module and the front end readout hybrids are glued to either side. After an internally and externally refereed review, the choice of microchannel technology was made for the cooling substrate implementation.

### 9.1 Requirements

The cooling solution for the VELO must satisfy the following criteria:

- Each module is equipped with twelve VeloPix, each expected to generate up to 3 W of heat. Furthermore, the ASICs for control and monitoring will dissipate an additional 5 W of heat. The inner sensor tiles, after irradiation are estimated to produce up to 1 W each. Hence the cooling substrate of each module must dissipate 43 W reliably throughout the lifetime of the experiment.
- Thermal run-away must be avoided with a clear safety margin, hence all parts of the silicon sensor must be maintained at  $-20^\circ\text{C}$ . This requirement is most critical for the innermost region of the sensor where the radiation damage and hence the leakage current is largest. In order to achieve this temperature at the sensor tip with a realistic CO<sub>2</sub> operating temperature, the smallest possible  $\Delta T$  ( $< 8^\circ\text{C}$ ) between the coolant and sensor is essential.
- These requirements mandate that active coolant runs in very close proximity to the ASICs, well into the LHCb acceptance. This brings a critical focus on the cooling technology choice because it must not only satisfy the stringent thermal requirements, but do so with the minimum material. The current VELO presents, on average, 20% of a radiation length to particles emanating from the interaction point with the dominant contribution from the RF foil. To provide competitive impact parameter performance the upgrade modules must contain minimal material. This places a stringent limit on the effective mass that the cooling solution may bring into the LHCb acceptance.
- The detector modules are located in a secondary vacuum, separated from the primary LHC vacuum by the RF foil which can withstand a differential pressure of 5 mbar.

No leaks from the cooling system are tolerated. In the failure scenario of a rupture in one of the modules, the differential pressure across the RF foil should not exceed 10 mbar.

- To avoid mechanical distortions after installation, it is advantageous to minimise the mismatch in coefficient of thermal expansion (CTE) between the various components of the module.

## 9.2 Microchannel cooling solution

The idea of passing cooling liquid through miniature channels etched within a silicon wafer is not new and many applications exist [38–40]. It is now gaining considerable attention as a technique for High Energy Physics applications [41, 42]. The principle of microchannel manufacture is to etch trenches into the surface of silicon wafer then atomic bond a cover wafer with suitable exit and entry holes such that liquid can circulate through the capillaries. To fabricate such a microsystem many steps are involved, including photolithography, etching, chemical mechanical polishing, bonding and dicing. The substrates may be silicon, plastic, or glass. For the VELO upgrade application both wafers in the final module are silicon. The trenches are etched to be 120  $\mu\text{m}$  deep in a 260  $\mu\text{m}$  thick wafer, such that when the 140  $\mu\text{m}$  thick cover wafer is bonded the channels sit symmetrically within the 400  $\mu\text{m}$  thick cooling substrate. Glass of various thicknesses has also been used as a cover wafer for several of the R&D steps, since samples can be produced without the need to go to industry<sup>7</sup> and have the advantage of allowing a clear view of the capillaries.

The advantages of the microchannel cooling technique address the requirements laid out above as follows:

- The cooling fluid circulates in direct contact with the silicon surface of the detector front end ASICs. The high thermal conductivity of silicon and the very small thermal barriers between the cooling and the heat source lead to a very high thermal efficiency.
- The choice of evaporative  $\text{CO}_2$  and bonded silicon is intrinsically radiation hard.
- The miniature channels have very small impact in terms of both mass and space. In addition, large local variations in material due to bulky cooling pipes are avoided in the active region.
- Due to the fact that the cooling substrate is in itself made of silicon, problems of CTE mismatch between cooling and heat source are avoided, aiding module construction.
- The production of the microchannel wafers proceeds with typical MEMS techniques readily available in industry. In principle it is possible to exploit this fact by adding additional features to the substrate such as traces for signal routing or precise double-sided alignment marks.

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<sup>7</sup>The samples used for the VELO R&D steps were produced at the micronanotechnology centre at EPFL, Lausanne, Switzerland.

The use of microchannel cooling with a single phase coolant has already been approved for the GigaTracker of the NA62 experiment [43]. The LHCb upgrade will be the first experiment to use a two-phase evaporative cooling system with boiling CO<sub>2</sub> in microchannels.

The pressure tolerance of the evaporative CO<sub>2</sub> microchannel cooling solution must be carefully scrutinised. The VELO upgrade operating pressure under normal conditions, when the detector is cold, is expected to be in the range 20 – 30 bar. In case of a failure the temperature and hence the pressure may rise, reaching for instance 60 bar at 22°C, and safety ratings are typically for 2.5 times this value. In the design of the cooling system, pressure-safety points (*i.e.* burst-disk) will be set at 100 bar and typically have 10% accuracy. The current VELO cooling system is rated at 170 bar.

### 9.3 Microchannel cooling R&D

The progress of this R&D project is summarised in this section.

**Proof of principle** In a laboratory test in 2012, boiling CO<sub>2</sub> was successfully circulated in a prototype microchannel network etched in 24 cm<sup>2</sup> pieces of silicon and bonded to a glass cover. The microchannel circuit, dubbed “snake” design, comprised 15 snaking capillaries 70 µm deep and 200 µm wide, set at 200 µm pitch. The prototype is shown in Fig. 61. The snake layout ensures that the channel lengths are reasonably similar. The inlet and outlet apertures were 2 mm diameter holes connected to plastic connectors glued to the silicon, reinforced with a steel plate. The channels emptied into a collector region in the silicon which was later found to be a point of weakness in the design. An important feature of this, and any microchannel network for evaporative cooling, is the implementation of *restrictions*: the first section of the circuit with a reduced microchannel cross section, just 70 µm deep × 30 µm wide in this case. The restrictions present high impedance in the circulatory system and ensure even flow across the downstream microchannels. A close up of the interface between the high and low impedance sections is shown in Fig. 61. At the end of the restrictions the sudden volumetric expansion of the sub-cooled CO<sub>2</sub> triggers boiling. This means that, if the coolant and the cooling circuit is correctly prepared, all the evaporative cooling power is concentrated where it is needed. This prototype was successfully tested with circulating CO<sub>2</sub> supplied by a mobile cooling plant which provided liquid CO<sub>2</sub> at -40°C with a pressure differential between the inlet and outlet of  $\Delta P \approx 4$  bar. A 6.8 cm<sup>2</sup>, 6.2 Ω heater was mounted to the silicon side of the circuit and four PT100 temperature sensors were mounted on the microchannel circuit as well as at the inlet and outlet. The complete microchannel assembly was operated in vacuum to emulate the conditions in the detector and to avoid condensation.

It was demonstrated that, with a  $\Delta P \approx 3$  bar and a CO<sub>2</sub> mass-flow of 0.15 g/s, 12.9 W of power could be removed from the module before the CO<sub>2</sub> was completely evaporated (referred to as a ‘dry-out’). The total heat removal was limited by the  $\Delta P$  which could be supplied by the cooling plant. At maximum heat dissipation, the temperature differential between the heater and the output was only 3 K. From this the thermal resistance  $\Omega_{\text{thermal}}$

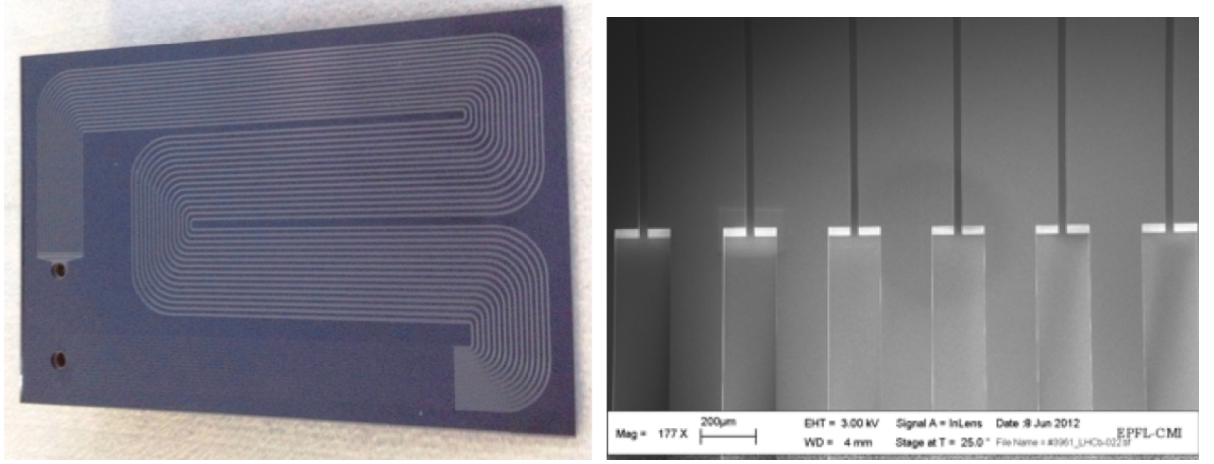


Figure 61: (left) The 2012,  $6 \times 4 \text{ cm}^2$  silicon-glass prototype. (right) The end of the high-impedance, restricted-width region where the evaporation is triggered in the larger volume.

of the system can be extracted to provide a figure of merit for the cooling performance. The measured value was

$$\Omega_{\text{thermal}} = \frac{\Delta T_{\text{heater-output}}}{\text{Power}/\text{cm}^2} = 1.5 \text{ K cm}^2 \text{ W}^{-1}$$

which is highly competitive. This work was published in [44].

**Wafer bonding processing** In a second R&D phase a large number of silicon-silicon samples (as opposed to the silicon-glass samples) were commissioned<sup>8</sup>. The samples featured a variety of channel pitches and dimensions in order to evaluate various aspects of the design. Sample sets from two different bonding processes were received, *hydrophilic* and *hydrophobic* which differ in the complexity of the surface preparation.

- The hydrophilic process is the industry-wide technique which introduces water molecules across prepared silicon surfaces and Si–OH hydrogen bonds form. Upon contact of the surfaces the Si–OH groups readily bind to each other forming Si–O–Si covalent bonds. These bonds increase in number and strength during an annealing (heating to  $800^\circ\text{C}$ ) during which the residual  $\text{H}_2\text{O}$  disperses in the crystal lattice.
- A hydrophobic process removes any oxide layer and allows direct Si–Si covalent bonding. The disadvantage is that the surface quality must be of a much higher standard and prepared in a higher-specification clean room, if voids (bubbles in the Si–Si bond) are to be avoided. The potential advantage is a near-perfect homogeneous union of the silicon lattice.

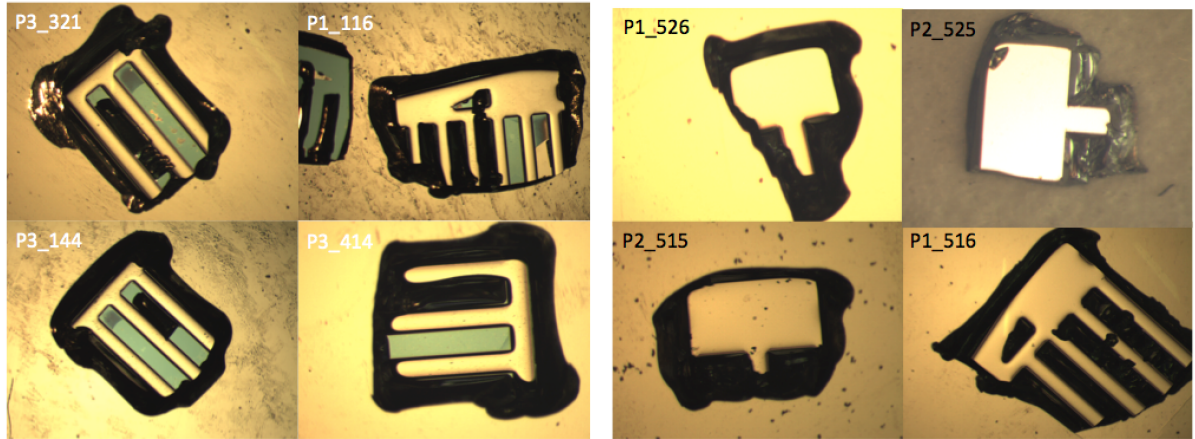


Figure 62: (left) Hydrophilic bonding ruptures. A small piece of silicon with dimension  $< 500 \mu\text{m}$  has been blown away exposing a few microchannels underneath. The shiny surface indicates that the break occurred in the fusion layer, and are associated with the Hydrophilic ruptures. (right) Hydrophobic bonding ruptures have a dark, uneven quality, indicating breakages within the silicon lattice.

Pressure tests have been performed (with water) on simple Si–Si microchannel samples produced with the two different bonding processes but with an identical range of designs with various channel pitches and sizes. The breakages which were provoked in the test samples occurred at the large output collector regions, which will not be used in the final design (see Sect. 9.5). Some typical pictures of the observed ruptures are shown in Fig. 62. The ruptures in the hydrophilic samples produce a clean ‘shiny’ surface indicate that the rupture occurred in the wafer bond. The hydrophobic bonding ruptures leave an uneven surface and break only at the ends of the microchannels, indicating that the rupture occurs within the wafer. Hydrophobic bonding seems to form a more reliable bond across all the surface.

**Pressure resistivity of silicon microchannels** To permit tests to the highest pressure, silicon-silicon samples were clamped to reinforce the fluidic connection such that the integrity of the microchannels could be pressure-tested in isolation. Hydrophilic samples rupture in the body of the microchannel network around 400 bar. The hydrophobic samples held the maximum pressure of the pump, 700 bar.

The dependence of the pressure resistance on the thickness of the silicon cover layer was investigated by the CERN PH-DT group and is reproduced in Fig. 63. In this study, rupture tests were performed on a number of samples of different silicon thickness and microchannel width. A clear relationship between rupture pressure and silicon thickness is observed for  $500 \mu\text{m}$  wide microchannels. The  $200 \mu\text{m}$  wide microchannels, which is the nominal width for LHCb, tolerate pressures of more than 200 bar even with a  $30 \mu\text{m}$  cover

<sup>8</sup>Following a tendering process the samples were produced at CEA-LETI, Grenoble, France.

layer. Note, however that this test investigates the effect of the silicon thickness, and not the performance of the bonding. For the nominal LHCb design thickness of  $140\text{ }\mu\text{m}$  the rupture pressure obtained by extrapolation is off the scale. This indicates that the fact that all hydrophobic samples hold 700 bar is in line with expectation for the given cover thickness.

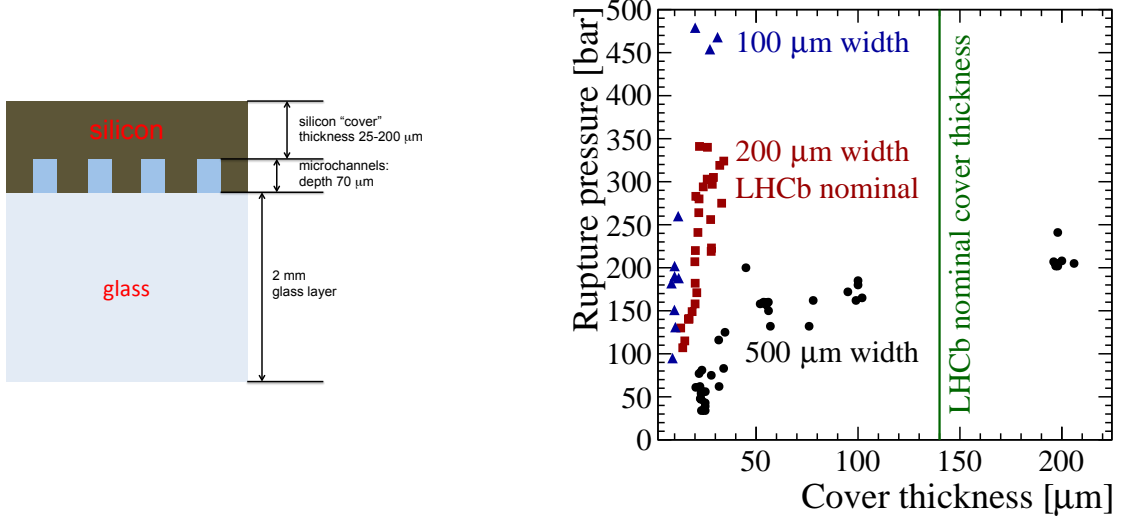


Figure 63: A study of pressure vs. the thickness of the silicon substrate enclosing the microchannel. For  $500\text{ }\mu\text{m}$  wide microchannels, a  $200\text{ }\mu\text{m}$  thick cover sustains about 200–250 bar. For  $200\text{ }\mu\text{m}$  wide microchannels, which is the nominal for the VELO upgrade, this pressure resistance is exceeded even with a  $25\text{ }\mu\text{m}$  thick cover, and for the LHCb nominal cover thickness of  $140\text{ }\mu\text{m}$  the pressure resistance as extrapolated from the red squares is so high as to be off the scale of this experiment.

**Endurance cycling** To stress-test micro channels, a laboratory system has been established to automatically cycle temperature and/or pressure. The pressure is supplied by a bottle of compressed air and the gas is heated by a Peltier unit with a glycol-based heat exchanger. A maximum pressure of 170–190 bar is possible and temperatures in the range  $-40$  to  $40^\circ\text{C}$ . Two Si-Si samples have been tested in this setup over a two month period during which they survived over a 1000 temperature cycles (each lasting 800 seconds) at a static pressure of 12 bar, and several thousand pressure cycles from zero to  $\sim 180$  bar at room temperature. These endurance tests are considered important milestones in validating the inherent long-term practical reliability of silicon microchannels.

## 9.4 Thermal mockup of a pixel module

The cooling performance has been evaluated using thermal mockups designed to emulate one half of one pixel module. Six ASICs and two silicon sensors are simulated with silicon



heaters. In nominal conditions the ASICs should generate 12 W total. However the cooling should tolerate up to a maximum of 3 W per ASIC, giving a total of 18 W. The heaters mimic the heat distribution in the ASICs, where the power is split roughly evenly between the main area of the ASIC and a narrow region at the back edge containing the high speed serialisers. The heat generated in the sensor is simulated by heaters with a concentric design aimed to mimic the  $1/r^2$  dependence of the particle fluence. The setup is illustrated in Fig. 64.

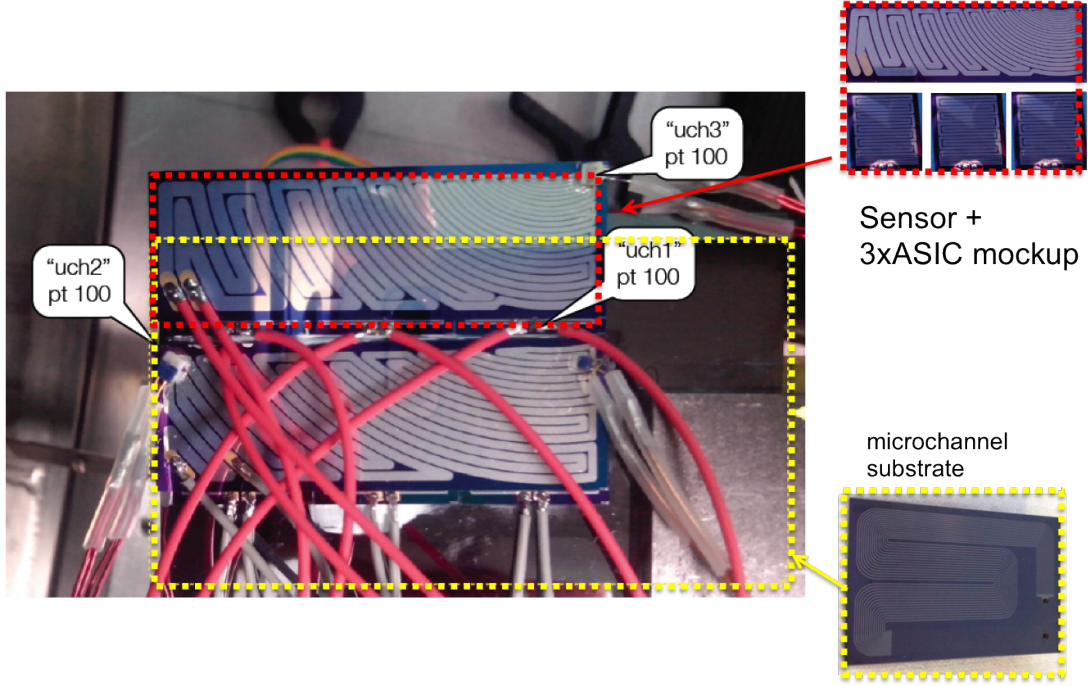


Figure 64: Experimental setup used to test cooling performance. Heater mockups are used to simulate the heat dissipation of the ASICs and irradiated silicon sensors. Cooling is provided by a microchannel substrate.

The heaters were attached to the snake sample with a cooling surface equivalent to that of one half module. Three temperature probes were positioned on the microchannels plus ASIC and sensor mockups. Most critically one sensor (labelled uch3 in Figs. 64 and 65) is placed at the tip of the mock-sensor. This is the point on the silicon which is closest to the interaction region but furthest from the coolant microchannel substrate, and hence the hottest spot on the module. During this test, the CO<sub>2</sub> unit provided a total flow of 1.2 g/s and a pressure drop  $\Delta P$  of 4.3 bar. A test in “nominal conditions” was performed with 11.5 W on the ASICs, and a gradually increasing power dissipation on the sensor, through the expected end of lifetime dissipation of  $\sim 1$  W. As can be seen in Fig. 65 the temperature increase on the uch3 sensor demonstrates a linear increase. The effective thermal resistance can be extracted from the slope and is measured to be  $\Omega_{\text{thermal}} = 7.20 \text{ Kcm}^2/\text{W}$  which remains very competitive. The measured  $\Delta T$  is approximately 6°C at end of lifetime. In a second test the ASIC heaters were operated at 20 W, which is above the highest expected

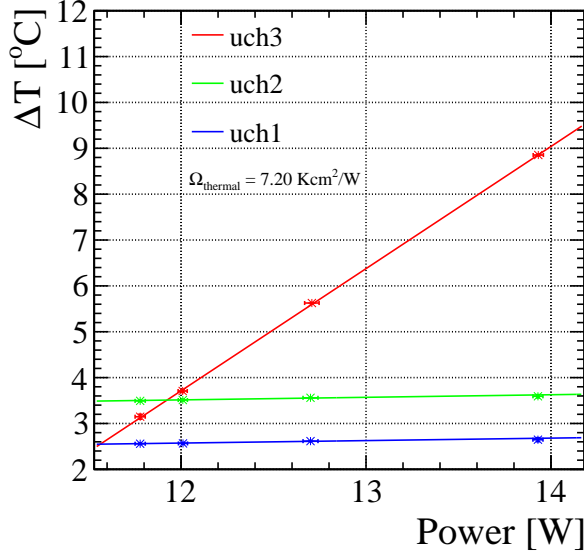


Figure 65: Measured temperature differential with fully powered ASICs and a gradual increase in power dissipation in the sensor. The end-of-lifetime expectation corresponds to a power dissipation of  $\sim 13$  W. The three colours correspond to three temperature probes; probe uch3 is located furthest from the microchannels and is hence the hardest point to cool.

power generation. The measured  $\Delta T$  remained at approximately  $6^\circ\text{C}$  for uch3. This is due to the effectiveness of the substrate at providing local cooling, and the fact that much of the ASIC power is concentrated at the part of the ASIC more remote from the silicon tip. These results indicate that the VELO upgrade sensors can be held below  $-20^\circ\text{C}$  assuming the flowing  $\text{CO}_2$  is provided at  $\sim -30^\circ\text{C}$ .

## 9.5 Channel dimensions and layout

All the proof-of-principle development detailed above used  $70\text{ }\mu\text{m} \times 200\text{ }\mu\text{m}$  microchannels at  $200\text{ }\mu\text{m}$  spacing. These initial choices have been revised for the final specification.

**Channel spacing** A finite element analysis has been used to quantify the heat flow through a microchannel substrate and to optimise the spacing between the microchannels. This study modelled a homogeneous  $400\text{ }\mu\text{m}$  silicon substrate containing  $70\text{ }\mu\text{m} \times 200\text{ }\mu\text{m}$  microchannels. A thin heat source on one side provides  $3\text{ W/ASIC}$  ( $\sim 36\text{ W}$  per module) as expected with the final pixel module. The study indicates that a separation of  $500\text{ }\mu\text{m}$  between channel edges is optimal, allowing efficient heat exchange along three sides of the channel, instead of being dominated by the side closest to the heat source which is the case for smaller pitches. In addition the larger spacing provides maximal bonding surface. With this design the simulation shows a negligible temperature differential between the coolant and heated surface, see Fig. 66. The full module under maximum power with a coolant temperature of  $-30^\circ\text{C}$  shows an expected  $\Delta T$  to the silicon tip of about  $7^\circ\text{C}$ , as illustrated in Fig. 67.

**Channel dimensions** With the microchannel system the critical factor is mass-flow of the coolant. This is in turn specified by the resistance of the network and the pressure drop



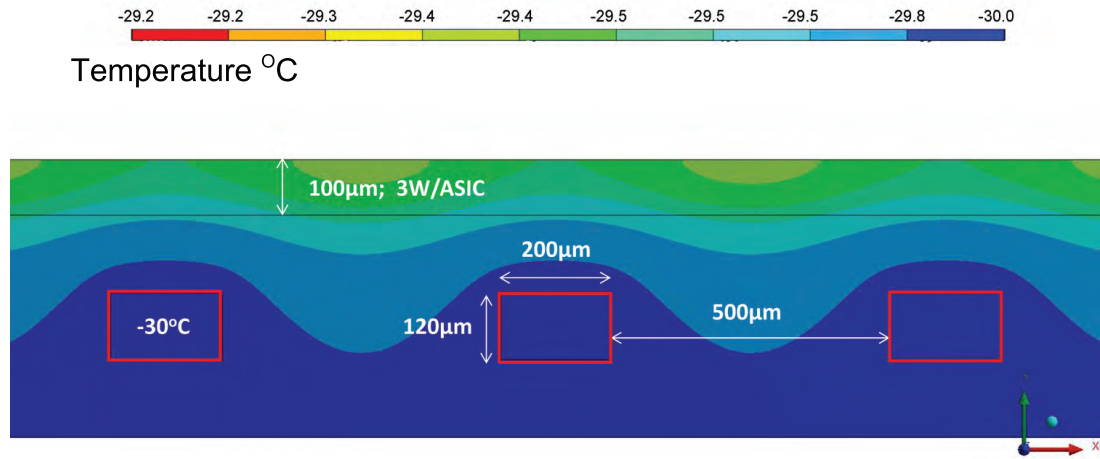


Figure 66: Thermal map from the microchannel FEA simulations, with a cross section illustrating the optimal channel separation and the very small temperature gradients to the heat source.

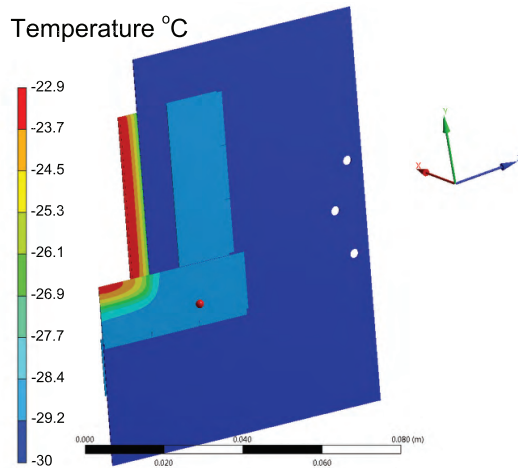


Figure 67: Thermal map from the microchannel FEA simulations, with a view of the full module with nominal heating. The maximum  $\Delta T$  to the silicon tip, from which the cooling substrate is retracted, is estimated to be about 7°C.

$\Delta P$  across the network that the cooling plant can provide which has proven a limiting factor for the small scale cooling plant used during the R&D phase. Following the impressive results of the mechanical integrity of the silicon substrate a study was performed into

the  $\Delta P$  dependence on the channel dimensions. It is concluded that by using a channel  $120\text{ }\mu\text{m} \times 200\text{ }\mu\text{m}$  with a  $60\text{ }\mu\text{m} \times 60\text{ }\mu\text{m}$  restriction in the initial section causes a sufficient reduction in flow resistance that the same mass-flow can be provided with a factor four reduction in required  $\Delta P$ . The consequential reduction in silicon above and below the channel is considered unproblematic. The move to a square restriction has the advantage that less turbulent flow is expected, at the cost of adding an extra step in the wafer etching process, due to the depth difference between the restrictions and main channels.

**Microchannel substrate layout** The microchannel layout is designed such that the main channels (where the  $\text{CO}_2$  boils) are routed under the pixel ASICs. The return path passes underneath the GBTx, SCA and GBLD ASICs. A single loop of 19 parallel channels is sufficient, with  $700\text{ }\mu\text{m}$  channel pitch in the main body of the cooling substrate. The total length of the network is around twice that of the snake R&D design, see Fig. 68.

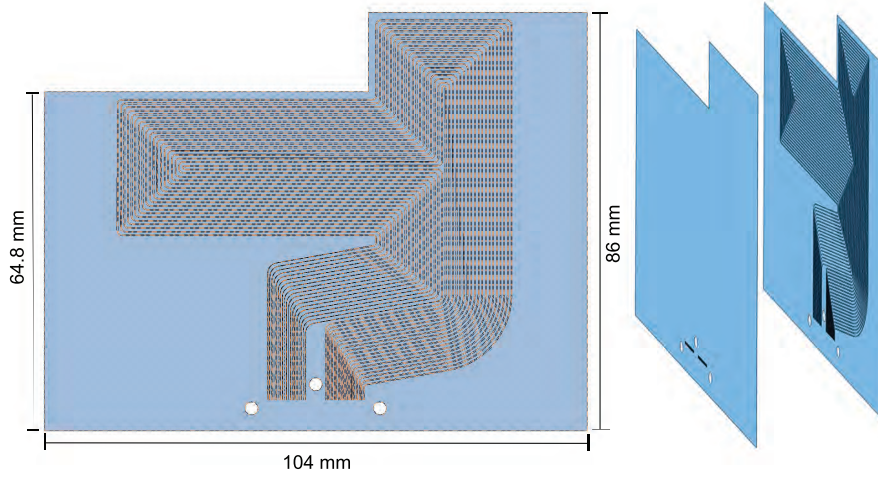


Figure 68: Microchannel layout for one module

## 9.6 Connector Design

The fluidic interface between the silicon and the  $\text{CO}_2$  supply is an important element of the microchannel design as it will reside inside the vacuum tank. The connector must deliver the  $\text{CO}_2$  to the microchannel substrate and collect the emerging boiling fluid. The conceptual design, shown in Fig. 69 unifies the input and output into a single unit. The incoming and outgoing cooling pipes, each of  $1.2\text{ mm}$  internal diameter, are inserted into either side of the connector and brazed into position. The liquid passes from the cooling pipes into a slightly narrower tube within the connector, then connects to the inputs of the microchannel substrate via long slits dubbed “slids”, from which an even flow is

distributed to the array of nineteen microchannels. The liquid accesses each microchannel via individual  $200\text{ }\mu\text{m} \times 600\text{ }\mu\text{m}$  openings in the cover layer. In this way the collector region within the silicon is avoided and the pressure resistance of the system optimised. The microchannel pitch is narrowed from  $700\text{ }\mu\text{m}$  to  $400\text{ }\mu\text{m}$  in the connector region, reducing the length of the slits to  $8.4\text{ mm}$  total. The design illustrated here is conservative and designed to be easily manufactured for prototyping purposes. The design described here, which is  $2.5\text{ mm}$  thick, introduces a total of  $2.4\%$  to the total material budget (see Fig. 19). It is anticipated that the shape can be profiled and the geometry changed to further reduce the material.

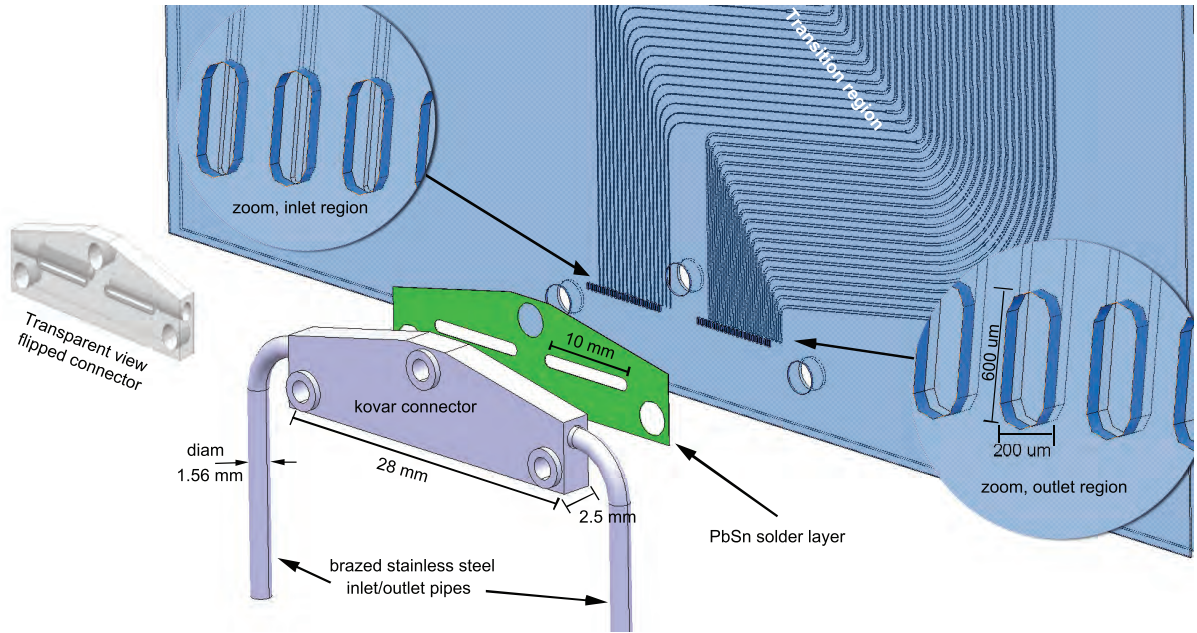


Figure 69: Schematic of the microchannel connector, showing details of the microchannel network at the point of attachment. The metallic connector partially enters the LHCb acceptance so must be kept as small as possible, and further optimisation is envisaged.

This connection cannot be secured with a clamp as this would place unacceptable mechanical stress on the  $400\text{ }\mu\text{m}$  thick silicon wafer. The proposed solution envisages a direct soldered bond between the silicon and a metallic connector, made of kovar (or possibly another alloy with CTE matching to that silicon.) The connector soldering procedure must satisfy the following criteria:

- a low temperature solder is needed such that the cooling pipes may be soldered with an equivalent high temperature adhesion.
- the solder must be leak-tight to several-hundred bar. This is most safely achieved if the solder footprint matches exactly the profile of the fluidic connector. This could

be achieved with the use of a preform, or by electroplating the solder. R&D tests on the former solution have so far proved very promising.

- when liquefied, the solder must not enter, or block, the microchannel aperture. In order to protect against this eventuality the width of the slid is currently widened to 1 mm, matching the 1 mm width slit in the preform, and there is an internal step in the slid within the connector to narrow it to match the internal cooling fluid tube. Based on the success of the tests so far this dimension may be narrowed for the final version.
- the procedure must be repeatable and uniform.

A number of soldering procedures are being pursued and the initial pull and pressure tests adhering brass connectors (for maximum CTE mismatch) and plain silicon samples have demonstrated that a normal low temperature PbSn solder reflowed in a vapour-phase oven is able to withstand 700 bar.

## 9.7 Cooling system architecture

The power and temperature requirements of the VELO upgrade are similar to that of the ATLAS Inner B-layer project. The design of the CO<sub>2</sub> cooling plant will closely resemble this proven design, which in turn has its origins in the current VELO cooling architecture.

The current VELO system contains two tertiary CO<sub>2</sub> cooling loops, each connected to an accumulator, which allows the temperature in the detector to be controlled via the system pressure. The loops are cooled by a water cooled chiller and there is a backup air cooled chiller. The cooling plant is currently operating close to the limits of what can be achieved in terms of power removal at operational temperature. The upgrade cooling plant will build on the experience gained with the current system and allow greater power dissipation at lower temperatures. It is currently considered advantageous to combine the VELO cooling with that needed for the LHCb upgrade UT subdetector [2] which will also use evaporative CO<sub>2</sub> cooling. In this way the resources can be shared between the two systems for construction, operation, and maintenance, at the expense of a small increase in complexity to allow safe and independent operation of two systems. Such a cooling plant would be designed with two independent CO<sub>2</sub> and freon (chiller) cooling racks. The chillers would be two-stage, with both water cooling and air cooling, allowing a full range of temperature operation. Based on previous experience and the knowledge acquired as the evaporative CO<sub>2</sub> cooling choice is now becoming more common, it is believed that the cooling plant will be successfully constructed, however the exact details of the location and architecture remain to be determined.

The upgrade VELO will be cooled by two tertiary CO<sub>2</sub> loops, one per half, as for the current system. The transfer lines to the detector might need re-routing, and a more efficient design is under consideration. The manifold making the connection to the vacuum tank, in addition to the internal routing of the capillaries (CO<sub>2</sub> distributor) up to the point where they will be welded to the modules must also be redesigned.

## 9.8 Cooling system safety

Much of the conceptual design of the cooling system, apart from the microchannel substrates and their fluidic connection, is either based on the current VELO design or that of related cooling projects, and therefore the risk is considered low. The part of the cooling system which resides within the secondary vacuum deserves special consideration because of the potential consequences of a sudden rise in pressure which could put the foil and/or the LHC primary vacuum at risk. The system risk must be assessed both for operational conditions, where the detector is under vacuum, and for shutdown conditions where the irradiated detector will be kept cold and the system will be flushed with Neon.

The principal risk is that of a destructive failure of a microchannel substrate or of a connector soldering, although our first pressure tests indicate a high level of robustness. A rupture would create a fast pressure increase in the VELO vacuum. The cooling system will be designed such as to minimize as much as possible the amount of CO<sub>2</sub> released into the detector vacuum in such an event. Several concepts and mitigations are being investigated such as the use of a dedicated exhaust volume outside the detector volume to mitigate the effect of an unwanted pressure rise in the distributor, the use of vacuum pressure detectors and mass spectrometry for fast CO<sub>2</sub> leak detection inside the detector vacuum, separation of individual module cooling lines, interlock valves, connector protection to prevent violent detachment in case of desoldering, etc. Extensive pressure/temperature cycle tests will be performed on the prototype and final modules, prior and after installation on the detector base. The validation procedure will be detailed in a separate document and externally reviewed in due time.

Another risk could be the blockage or gradual clogging of a restriction channel by impurities or slow deposition of a substance in the substrates, although no problem of this nature has so far been observed in the R&D phase. Due to the parallel nature of the cooling system a blockage of an individual channel would not have a large impact. Long term pressure and temperature cycling tests will help to understand if any such effect can be expected. The final system will be equipped with filters which are able to remove particles down to a few microns in size. Because of this, it is unlikely that debris will block the microchannels whose narrowest aperture is the  $60 \times 60 \mu\text{m}^2$  restriction. Furthermore, regular monitoring of the pressure drop across the system and analysis of the CO<sub>2</sub> flowing in the circuit should reveal the presence of any contaminant.

For the currently installed VELO a risk assessment was carried out [45] which addressed the possible release of CO<sub>2</sub> in the secondary vacuum and the role of the valve protection system which acts to maintain a maximum of 5 mbar differential pressure between the primary and secondary volumes. This risk assessment will be updated and a review process organized with the LHC vacuum group to take account of the major changes in the system, *i.e.* the use of a new technology for the cooling distributor and substrate.

## 10 Mechanics

The VELO modules are housed within a 1.4 m long, 1.1 m diameter cylindrical vacuum tank co-axial with the beam pipe. The tank allows the sensors to operate close to the beam and caters for two important requirements; first it permits the sensors and any passive material to be moved to a safe position during injection and, second, it provides separation between the primary machine vacuum and the secondary vacuum in which the sensors are operated. The upgrade will reuse the existing VELO tank, shown schematically in Fig. 70. The detectors will again be mounted in two halves parallel to, and on opposite sides of, the nominal beam axis.

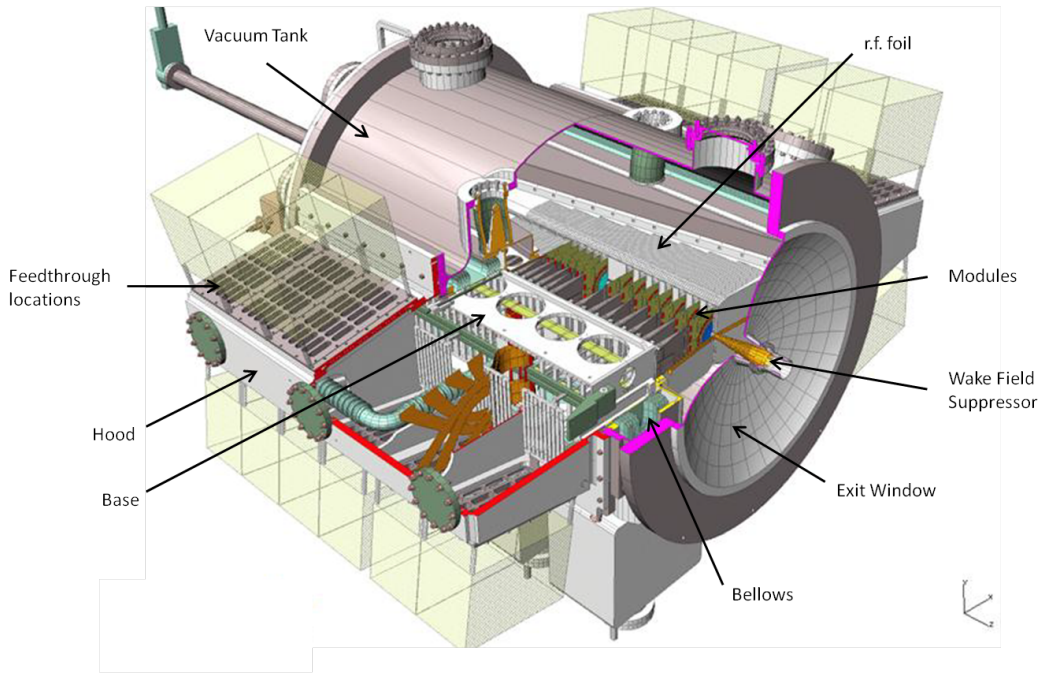


Figure 70: A schematic view of the existing VELO tank and key components.

The tank houses several key components: two bases, one for each half, on to which modules are mounted; two corresponding RF foils which provide a thin, leak tight barrier between the vacuum regions and which also act to shield the sensors from noise induced by the pulsed structure of the beam; a bellows system that permits each detector half to move independently in  $x$  whilst retaining the vacuum seal; a wake field suppression system which ensures a smooth transition of beampipe diameter, as seen by the beams, and which must therefore also move with each half independently; the cables which supply the LV and HV to the modules; the high speed electrical links which will be used to transmit the data from the modules and the distribution of the CO<sub>2</sub> cooling. At the downstream end a large, thin, aluminium window permits particles to exit the VELO tank through minimum material.



To the tank are attached two hoods. The hoods seal the large access apertures which are used to insert the VELO halves. The hoods also locate the vacuum feedthroughs that carry the control and data signals in and out of the tank and the ports for the CO<sub>2</sub> coolant. On the hoods are mounted the Opto and Power Boards (OPBs) which transmit the data from the front end to the off-detector electronics and beneath the tank is the system that drives the motion of the VELO halves. The control systems for motion and cooling are located 60 m away, behind the shielding wall, and are accessible during LHC operation.

The upgrade will require design changes to the VELO mechanical system and a new installation procedure; a summary of the major items is given below.

## 10.1 RF foil

The foils must satisfy a number of conditions for the LHC: they must provide good vacuum conditions in the presence of beam; electrical continuity along the beam direction and not significantly contribute to the impedance of the machine. The experimental requirements are to bring the foil as close to the beam as possible and to reduce its thickness to a minimum. These are major objectives for the upgrade and have been shown, see Sect. 4.4, to have a major effect on improving the impact parameter resolution. A distinctive feature of the upgrade is the replacement of the existing ‘toblerone’ shape with a stepped L-shape design, see Sect. 3.1.2 and Fig. 71.

The RF foils can be described as large rectangular boxes ( $\approx 1 \text{ m} \times 0.2 \text{ m} \times 0.4 \text{ m}$ ) with one of the two long faces removed and where the opposite face, which mates closely with the other detector half, has a complex corrugated structure. Two conflicting requirements make their construction extraordinarily difficult: first they must be light, typically with a thickness of  $\mathcal{O}(\leq 250 \mu\text{m})$  of AlMg<sub>3</sub> and second they must be leak tight to preserve the quality of the LHC UHV at the interaction point. Furthermore, the boxes must be constructed with tight tolerances to allow the two detector halves to come together. They must also withstand radiation doses of up to 1000 MRad in the regions closest to the interaction point. The requirement to place the sensors as close to the beam as possible means they will be, by necessity, in close proximity to the box. Should the sensors touch the foil, or come sufficiently close for an electrical arc to develop, severe damage could result.

The tight dimensional tolerances result in the need for dimensional stability. This is complicated by several factors: the temperature of the box will depend on whether the LV is on or off because of radiative heating from the FE electronics; the DAQ configurations; the image current from the beams and the status of the cooling. Changes of  $\mathcal{O}(1^\circ\text{C})$  are observed in the current detector due to their open/closed configuration. Prior to LS1 increases in the foil temperature of  $0.7^\circ\text{C}$  at a beam current of 0.35 A were measured; with a current of up to three times more (in HL-LHC) the temperature increase could be up to 10 times higher. We require the new RF foil must not exceed its dimensional tolerances for temperature differences of  $10^\circ\text{C}$  corresponding to an approximately  $200 \mu\text{m}$  change in 1 m of aluminium. Furthermore the foil must be designed to withstand operational differential pressures of 10 mbar during its lifetime and allow for the application of a Non-Evaporable

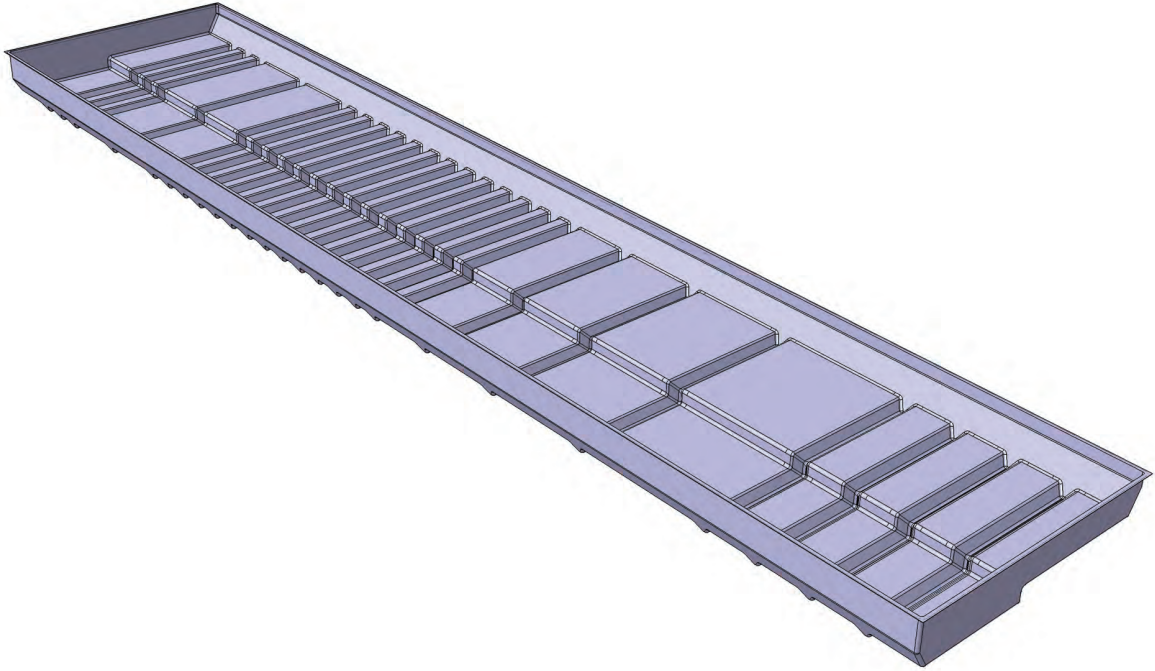


Figure 71: The design of the beam-facing side of the full size RF box. The side walls are approximately  $500\text{ }\mu\text{m}$  thick, the corrugated section will be  $250\text{ }\mu\text{m}$  thick and, close to the beam axis, may be thinned still further.

Getter (NEG) coating, on the beam facing side, which requires activation at temperatures above  $160^{\circ}\text{C}$ .

### 10.1.1 Manufacturing technique and prototypes

The current manufacturing technique involves hot gas formation of the corrugations on a flat piece of thin aluminium and then welding this piece and the remaining four sides together, and then to a flange, to complete the structure. This is a laborious and complex process which was difficult to reproduce for the original foil shape and impossible to fabricate with the new design.

For the upgrade it is proposed to produce the box by milling a solid block of aluminium-magnesium alloy. First the outside profile is milled which is subsequently placed in a mold and evacuated, after which the inside is milled. The milling process offers clear advantages. The shape that is produced is cut at room temperature and can be measured during production using an instrumented arm on the milling machine, obviating some of the problems associated with hot gas forming. Perhaps more importantly the need to weld the sides of the box to the flange is entirely eliminated, as the flange and four sides may be cut from a block also.



Small prototypes of the foil have been built. An example of a recent prototype is shown in Fig. 72. The milling process is such that it is difficult to reliably reduce the thickness of the aluminium to less than  $250\text{ }\mu\text{m}$  over the full length of the box. As it remains highly desirable to further reduce the thickness, progress has been made on developing a chemical etching process using sodium hydroxide. Using this method the thickness of the foil may be reduced, evenly and repeatedly, by over  $100\text{ }\mu\text{m}$ , see Fig. 73. Ignoring any other issues the thickness of the foil should not be reduced beyond  $\mathcal{O}(100\text{ }\mu\text{m})$ .

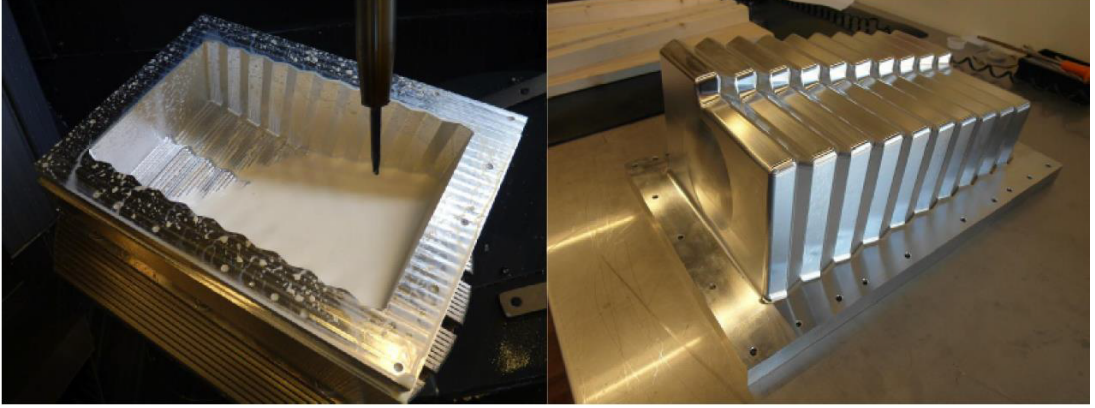


Figure 72: (left) A photograph of an aluminium block being milled. (right) the finished prototype. The walls are approximately  $500\text{ }\mu\text{m}$  thick, the corrugated top section is approximately  $300\text{ }\mu\text{m}$  thick.

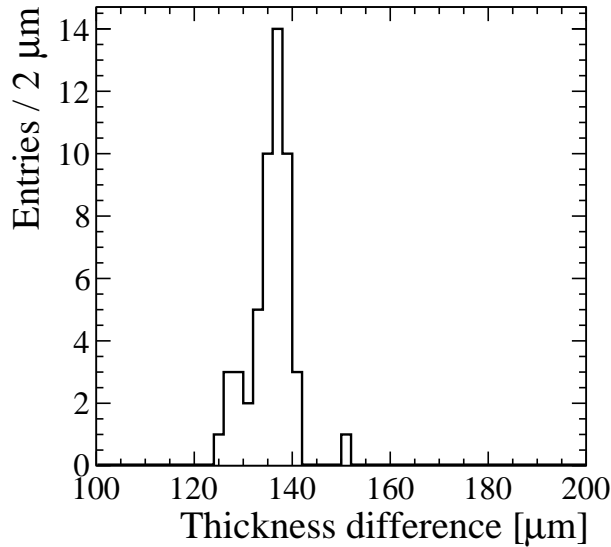


Figure 73: Typical distribution of the etched-away thickness for a sample  $300\text{ }\mu\text{m}$  aluminium RF foil. The thickness was measured on a trajectory across a corrugation before and after etching. The histogram shows the difference between these two measured thicknesses. The average thickness of the foil has been reduced to about  $160\text{ }\mu\text{m}$  with an RMS of  $19\text{ }\mu\text{m}$ .

## 10.2 Detector base and hood

Two major components of the mechanics that must be replaced for the upgrade are the detector bases and the hoods. We discuss each separately below.

### 10.2.1 Base

The bases contain the locating slots that permit the precise placement of the modules onto their mechanical support. These in turn are mounted on the centre-frame of the VELO and a motion system which permits the movement of both halves. The two bases, one for each side, are of almost identical design but are differentiated along the beam direction ( $z$ ) by their slot positions. These are staggered to allow the detector to bring the two halves as close together as possible. Otherwise the new bases will be manufactured to correspond closely to the existing base design (see Fig. 74) including an integrated heating system allowing for thermal stabilization of the base to  $\pm 1^\circ$  around  $20^\circ\text{C}$ .

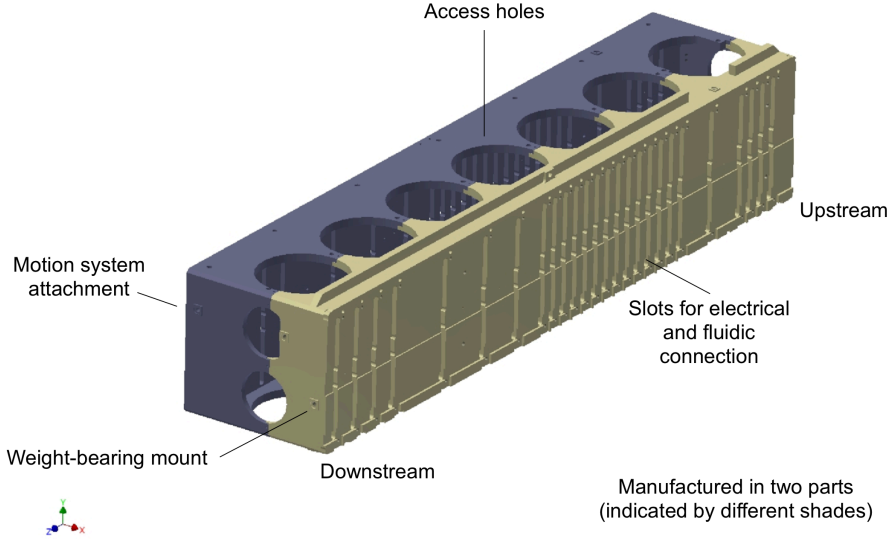


Figure 74: Drawing of the VELO-C base for the optimised layout documented in Table 4.

Two further modifications in the bases are foreseen. The first is that the new module positions imply the ‘cutaways’ in the sides of the bases, there to permit easy access to the cavity under the modules, must also be redesigned. The second is to integrate easy-access stress relief clamps into the base underneath the modules. The clamps are necessary as the data and LV/HV supply cables will exert significant force on the modules due to both motion and thermal expansion. The bases will be engineered to permit the optional addition of a constraint system to restrict the movement of the modules in  $z$  due to the thermal expansion of the cables between the base stress relief system and the modules and to dampen vibration during transport. It may, in addition, prove necessary to design

a cooling pipe restraint system, attached to the base, to reduce stress on the delicate microchannel substrate cooling connectors.

### 10.2.2 Hood

The hoods seal the apertures through which the VELO halves are installed, see Fig. 70. The hoods separate the secondary vacuum in which the modules operate from the atmosphere. These are well out of the detector acceptance hence they can readily be engineered to withstand the stresses from differential pressures and from the cables (which are very stiff) connected to the module bases.

One of the most critical functions integrated in to the hood design is the routing of the CO<sub>2</sub> coolant from outside to inside the tank and the provision of feedthroughs that permit control signals, LV and HV supplies and data signals to pass in and out of the tank. New hoods will be fabricated which accommodate the new cable/feedthrough needs of the pixel system (see Sect. 7.3.3).

If the hoods are to remain in a fixed position relative to the tank, the cables and CO<sub>2</sub> supply pipes must take up the movement of the bases. In this case, to avoid the introduction of a new set of bellows, an additional stress relief system, for the supplies, will need to be installed on the inside of the hood. An engineering feasibility study will need to be performed to evaluate if the cables and pipes can be routed so as to overcome issues of fatigue and failure within the secondary vacuum.

It is proposed that the new hoods will allow the electronics to be mounted ‘horizontally’ rather than in the upwards/downwards orientation as on the existing tank. The option now also exists to bring the CO<sub>2</sub> coolant into the tank through individual pipes mounted in the same plane as the data and HV/LV supply feedthroughs on the hood.

### 10.2.3 Feedthroughs

One of the expensive items in the construction of the original VELO tank was the purchase of high quality high vacuum feedthroughs qualified by the manufacturer to standards acceptable by the LHC. For the upgrade HV/LV feedthroughs of the correct specifications may be purchased however there are no ‘off-the-shelf’ data feedthroughs which match the VELO requirements. The experiment must therefore develop custom feedthroughs, which minimize impedance mismatches, and at the same time may be qualified for operation at the LHC. One method under consideration is the ‘potting’, with UHV compatible compound, of short lengths of the data cables connectorised at each end.

The CO<sub>2</sub> may also be routed through the hood via separate feedthroughs. The advantage of this system is that it would allow the cooling to each module to be turned off outside of the tank should any leak develop. The risk is the introduction of  $\mathcal{O}(100)$  additional small feedthroughs in the vacuum system which will require additional welding and *in situ* quality control.

## 10.3 Assembly and transport

The existing VELO mechanics were fabricated at Nikhef and transported to IP8 for installation around the beam pipe. The exception was the population of the bases with modules which was performed at the CERN Meyrin site. There the detectors were electrically and thermally tested, and the positions of all the modules measured on the bases, prior to final transport to IP8.

The following summarizes the changes seen in the procedures for the pixel system. The largest change is the proposal to perform all the mechanical assembly of the halves remote from CERN, and then transport the fully tested halves directly to IP8 for installation.

### 10.3.1 Assembly method

The components required to build the VELO halves have been described above (modules, cables, bases, hoods). These will be brought together at the assembly site which must provide: vacuum testing, a CO<sub>2</sub> cooling system, thermal imaging, a DAQ slice, HV and LV supplies, and metrology infrastructure.

Additional mechanical components which are required will be modified and reused from previous VELO builds, for example: trolleys which hold the detector halves during assembly; and vacuum testing covers which fit onto the hood flange, where the seal would be made to the tank, to permit the modules to be tested under vacuum.

The VELO group has developed an automated quality assurance database which follows every component through each step of the production process and asserts production control. This is one of the key elements of the success of the strip-detector VELO. Originally developed for module production only this has already been extended to the full assembly of the replacement VELO and will be again extended for the pixel VELO upgrade.

All components received at the assembly site will be undergo metrology to ensure conformance with production specifications and visually inspected for damage during transport to the site. Small reflectors or spheres will be glued to the base and measurements made with an optical (Faro) laser tracker compared with contact measurements. Studies performed by the group indicate that over a volume of dimensions similar to the VELO the laser tracker has an accuracy  $\approx 2 \mu\text{m}$ , compared with the nominal  $15 \mu\text{m}$  specification.

The base and hoods, and internal mechanics, will be assembled together onto the trolleys together with the CO<sub>2</sub> distribution manifolds (distributors). We assume the distributors have been cleaned, inspected and qualified prior to shipping to the assembly site. The modules will then be mounted individually onto their bases.

A new feature of the module design is that cooling pipes/tails now form a part of the module as delivered to the assembly site. These cooling pipe/tails must be welded *in situ* to the main cooling manifolds which are to be provided together with the bases. This presents a challenge in several ways. Foremost is the issue that the tails will be delicate, as will the connections to the silicon microchannel substrate. Our assumption is that zero lateral, or normal force must be exerted on the connectors to avoid danger of cracking the thin silicon (almost at its point of maximum brittleness). Second if any pipe cutting or cleaning is to be performed on either opening of the pipes prior to welding then utmost

care must be taken not to permit the entry of any detritus into the pipes as this could block the microchannels.

The welding process itself must not contaminate the modules nor electrically damage the ASICs. The welded joints will be leak tested and be scanned with a portable x-ray system to ensure even quality of the weld. The cooling pipe support/ stress relief system must then be attached to this module. The modules, also equipped with retro-reflectors (or small glass spheres), can then be rapidly metrologized.

After each module has been attached to the base and cooling pipes welded, the electrical cables must be attached to the feedthroughs on the hood and to the modules; these semi-rigid cables must then be themselves attached to the stress relief mechanism integrated into the detector base and another point closer to the module pedestal and finally to the clamping system on the hood. Without forced cooling the module can then be readout during short runs  $\mathcal{O}(10\text{ s})$ .

After all the modules are mounted, a He leak test will be conducted on the completed half. Further to the He test, the detector half will be capped with a vacuum hood, and the entire volume evacuated whilst the modules cooling system is pressurized to twice the maximum nominal room temperature operating pressure of the system *i.e.* to approximately 150 bar. Following successful leak and pressure testing of the completed half, the system will be connected to a recirculating CO<sub>2</sub> system. This will permit testing of all the modules, under vacuum and whilst cooled to nominal operating temperatures. At this point multiple modules will be operated simultaneously. A test foil will be installed on each half, in close proximity to the modules, to check for coherent noise induced by inter-module coupling via the foil. Barring any failures the system would then be prepared for transport to CERN.

### 10.3.2 Transport

Transport of the two detector halves from a remote assembly site to CERN is a challenging but not insuperable task. The Endcap-C for the ATLAS SCT was transported to CERN, by road, without the failure of any components. The Endcap was a much more delicate structure than the upgraded VELO detector and, by virtue of size, much more cumbersome. Nonetheless extreme precautions will be taken to avoid any damage to the VELO halves.

The detectors will be fitted with a lateral constraint system, which could also be used in the experiment if necessary, but whose function is to restrict vibration of the modules in the  $z$  direction. The entire (encapsulated) halves will be fitted into individual transport containers. These containers will be fixed to the vehicle and will be equipped with shock absorbing systems which will provide critical damping in three dimensions and disallow any rotational oscillations. The boxes will be fully equipped with shock logs and accompanied at all times by physicists monitoring the vibrations. The boxes will be precision loaded on an air-ride truck; similar to the vehicle used for ATLAS. Qualification tests for the transport will include shock analysis over rough roads at 70 km/h with the boxes equipped with dummy loads and an analysis of the impact of emergency braking at a dedicated facility.

### 10.3.3 Reception

The detectors will be transported directly to IP8 in readiness for installation into the detector. After unloading the truck, the detectors in their containers will be transferred to an underground VELO reception area using the crane at the access shaft. The reception area must be a dust-free zone (comparable to ISO-7) and large enough to permit storage of both halves and a repeat of the metrology of the detector halves using the laser tracker. Only basic electrical checks on the modules are foreseen at this point. Following inspection and measurement the detector halves will be prepared for installation.

## 10.4 Installation sequence

Prior to installation of the new detector halves a large amount of work must be performed to safely extract the existing (activated) detector halves and to remove the existing RF foils which may be dismantled via the aperture opposite the VELO exit foil. During this preparatory phase not only must the existing VELO be removed but also key re-usable elements, such as the bellows, must be checked for signs of mechanical failure. Removal of the existing VELO will necessitate the re-installation of the overhead mounting track used to smoothly bring/remove the detector halves to/from the interaction point.

Once the existing components are qualified for re-use at the upgrade the new foils, probably NEG coated on the beam facing side, must be installed. Just before installation the LHC volume will be baked out and the NEG coating activated. Post bake-out/activation the interior of the foil will be remeasured to ensure that no distortion of the foil has taken place.

The two halves will then be brought, via the overhead ‘railway’, to the interaction point. The transport trolleys will then be removed for the final time, and the detector halves rotated and slid into position. A major step in the installation process is then completed by the sealing of the hoods to the VELO tank. The electronic and CO<sub>2</sub> connections will be made and the detector will then be ready for the next step in commissioning.

## 10.5 Vacuum and motion control systems

Two further subsystems deserve special mention and discussion, the vacuum and motion systems and their corresponding controls. Both of these systems are critical to the functioning of LHCb and, should a malfunction occur, could have a profound impact on the whole of the LHC. The vacuum system provides the monitoring, pumping and the control necessary to limit the differential pressure between the primary and secondary foil; maintaining the differential pressure is critical during the period where the LHC volume is filled with neon at atmospheric pressure. The motion system is responsible for the movement of the two halves allowing them to be carefully positioned around the luminous region and permitting the detectors to be retracted to their safe position whenever necessary.

Both systems will require refurbishing and key components replacing to ensure continued operation and the availability of spare parts until 2030. Special attention will be given to

ensuring that leak detection and failure mode safety systems are in place to protect the LHC in case of rapid decompression of the module coolant.

However the replacement of these systems will form part of the maintenance of the current VELO as the subsystems will, in any case, reach the limit of their operational life expectancy by about 2018 *i.e.* they require renewal irrespective of the upgrade. Hence they will not be described further here; we note their replacement will be financed by the existing detector maintenance and operations budget.

## 10.6 Timeline for mechanics

The major milestones for the mechanics of the detector are driven by the requirements to be prepared for installation *as soon as is practical* after the beginning of LS2 (January 2018). After leaving sufficient time to permit close proximity access to the VELO tank, the existing detector will be removed in Q2, 2018. The tank and ancillary/support equipment will be prepared for insertion. It is foreseen to provide a ‘green light’ for installation by Q4, 2018.

To meet this green light date the collaboration foresees an Engineering Design Review (EDR) of all the mechanics elements in Q3 2015 followed by a Production Readiness Review (PRR) of these components in Q2 2016.

## 10.7 Safety

All work conducted at CERN, in preparation and during the installation, and for the periods of commissioning and operation of the VELO will comply with CERN safety regulations. The VELO will require particular attention to: the radiological hazards during the de-installation of the existing VELO and its replacement with the upgraded detector, and attention to damage avoidance during (de)-installations. The group will conduct an initial safety review as part of its Engineering Design Review and a separate Safety Review will be conducted by CERN prior to start of decommissioning.

## 11 Project organisation

The LHCb upgrade is managed by the Upgrade Coordinator, who convenes the Upgrade Steering Panel. The VELO Upgrade is managed by the VELO Upgrade Coordinator and falls under the responsibility of the Tracker and Tracking representatives in the Upgrade Steering Panel, and also forms part of the VELO project. Within the VELO upgrade there are seven working group coordinators, who take responsibility for the following aspects of the project:

- **Software**, including detector and foil geometry description, FE response, alignment, pattern recognition and track reconstruction, testbeam software development and physics performance.
- **Electronics** including overview of system architecture, signal chain via electrical data links, feedthroughs, electrical to optical conversion, power distribution, controls and interlocks.
- **DAQ Integration**, including signal chain from TELL40 board with VELO specific firmware and software, VELO specific ECS components and testbeam support.
- **VeloPix**, including overview of Timepix3 and VeloPix design, production and characterisation.
- **Pixel Module**, including sensor, front-end hybrid and ASIC-sensor tile R&D and prototyping, and the integration of flex, substrate and support structures, thermal simulations, bench testing and QA procedures
- **Cooling**, including production and qualification of module cooling substrate, CO<sub>2</sub> distributor, cooling plant and transfer line development, integration with LHC vacuum group.
- **Mechanics**, including design and production of RF foil, detector base and hood, integration of electrical and mechanical feedthroughs, assembly and transport, vacuum, motion and control system.

### 11.1 Participating institutes and responsibilities

The institutes currently working on the VELO upgrade are listed in Table 14. The UK institutes have formed a joint project plan and assume collective responsibility for the relevant aspects of the project, pooling resources where necessary. Similarly the Dutch institutes represent a joint venture. In view of this these institutes are referred to as UK and Nikhef/VU in the remainder of this section.

The sharing of the main project tasks is listed in Table 15. The responsibility for developing VELO specific software concerning the DAQ, control and monitoring are included in the corresponding items. Development of the relevant reconstruction software,



Table 14: List of institutes actively contributing to the VELO upgrade project.

Country	Institutes
Brazil	Universidade Federal do Rio de Janeiro (UFRJ)
Ireland	University College Dublin (UCD)
Poland	AGH University of Science and Technology, Kraków
Russia	SINP, Moscow State University (MSU)
Spain	Universidad de Santiago de Compostela (USC)
Switzerland	CERN
The Netherlands	Nikhef
	Vrije Universiteit (VU), Amsterdam
United Kingdom	University of Bristol
	University of Glasgow
	University of Liverpool
	University of Manchester
	University of Oxford
	University of Warwick

including pattern recognition, detector description, and track fitting forms part of the mandate of the LHCb Tracking and Alignment Group, to which the VELO upgrade group contributes. The detector section includes development and production of silicon sensors, flip chipped tiles, front-end hybrids, module cooling substrate, and assembly and integration. The electronics section includes development and production of all VELO specific elements starting from the front end, through the complete data transmission and control chain, including items such as LV and HV distribution and interlock systems. The mechanics and infrastructure section includes development and production of the RF foil, detector bases, vacuum, cooling, motion and installation. All institutes are actively involved in the design and optimisation stage currently taking place, and contribute to system tests and quality control.

The exact distribution of responsibilities can only be finalised when the results of the requests to the funding agencies have become clear, hence the table represents the intentions of the institutes at the time of writing this TDR. The listing of institutes next to a task indicates the intention of those institutes to contribute fully or partially to that task.

## 11.2 Schedule

The upgraded VELO detector is scheduled for installation in Q4 2018, and the schedule in Fig. 75 displays the major activities from the publication of this document up to installation. Removal of the currently installed VELO detector is expected to occur in Q1

Table 15: Project sharing of responsibilities. The institutes (or group of institutes) listed for each task make a full or partial contribution to that task.

Task	Institutes
<b>Software</b>	All contribute
<b>Detector</b>	
Sensor tiles	UK, UFRJ, USC
Front-end hybrid	UK
Module cooling	UK
Component assembly, QA, integration	UK, Nikhef/VU
<b>Electronics</b>	
Front-end ASIC	Nikhef/VU, CERN
Optical & electrical links	UK, USC
LV and HV system	UK
DAQ integration and ECS	UK, UFRJ
General electronics	UK, MSU, UFRJ, USC
<b>Mechanics and infrastructure</b>	
RF foil and WF suppressors	Nikhef/VU
Detector base, hood, CO <sub>2</sub> distributor	UK
Vacuum, cooling, motion	All contribute
Installation and infrastructure	UK, CERN
<b>General</b>	
Detector design & optimisation	All contribute
Testbeam	All contribute
System test & commissioning	All contribute

2018. It is expected that commissioning of the installed upgrade VELO will extend into mid 2019.

A sensor R&D program, including irradiations, is planned for early 2014, the results of which will be documented at the sensor EDR in Q3 2014. The corresponding sensor PRR will take place Q2 2015.

The electronics EDR is scheduled for Q3 2014 at which occasion the hybrid, electrical high speed link as well as the opto and power board will be reviewed.

The first submission of the VeloPix chip is scheduled for Q3 2014. After a successful verification process the electronics PRR will take place a year later, *i.e.* in Q4 2015.

The thermo-mechanical design of the module and the R&D of the cooling substrate will culminate in the module EDR in Q1 2015. After a year of module prototyping the module PRR will be held in Q1 2016.

In Q1 2015 a review of the functionality and architecture of the FPGA-code will take place. In Q1 2016 the first version will be operational, such that it can be used in the tests of the firstly produced modules.

The investigation of the possibilities to upgrade the cooling plant will be evaluated in Q4 2015.

Safety aspects will be reviewed individually, generally with an initial safety review in the corresponding EDR and a final safety review in the corresponding PRR. Specifically, cooling system safety will be reviewed in the Module EDR and PRR in Q1 2015 and Q1 2016, respectively. Mechanical safety aspects will be covered in the Mechanics EDR and PRR in Q3 2015 and Q2 2016, respectively.

There is a strong interplay between the design specifications of the cooling substrate and module, module and detector support as well as all these items and the RF foil. Consistent design tools and archiving rules will be implemented, such that regular integration meetings can guarantee a smooth design and production process.

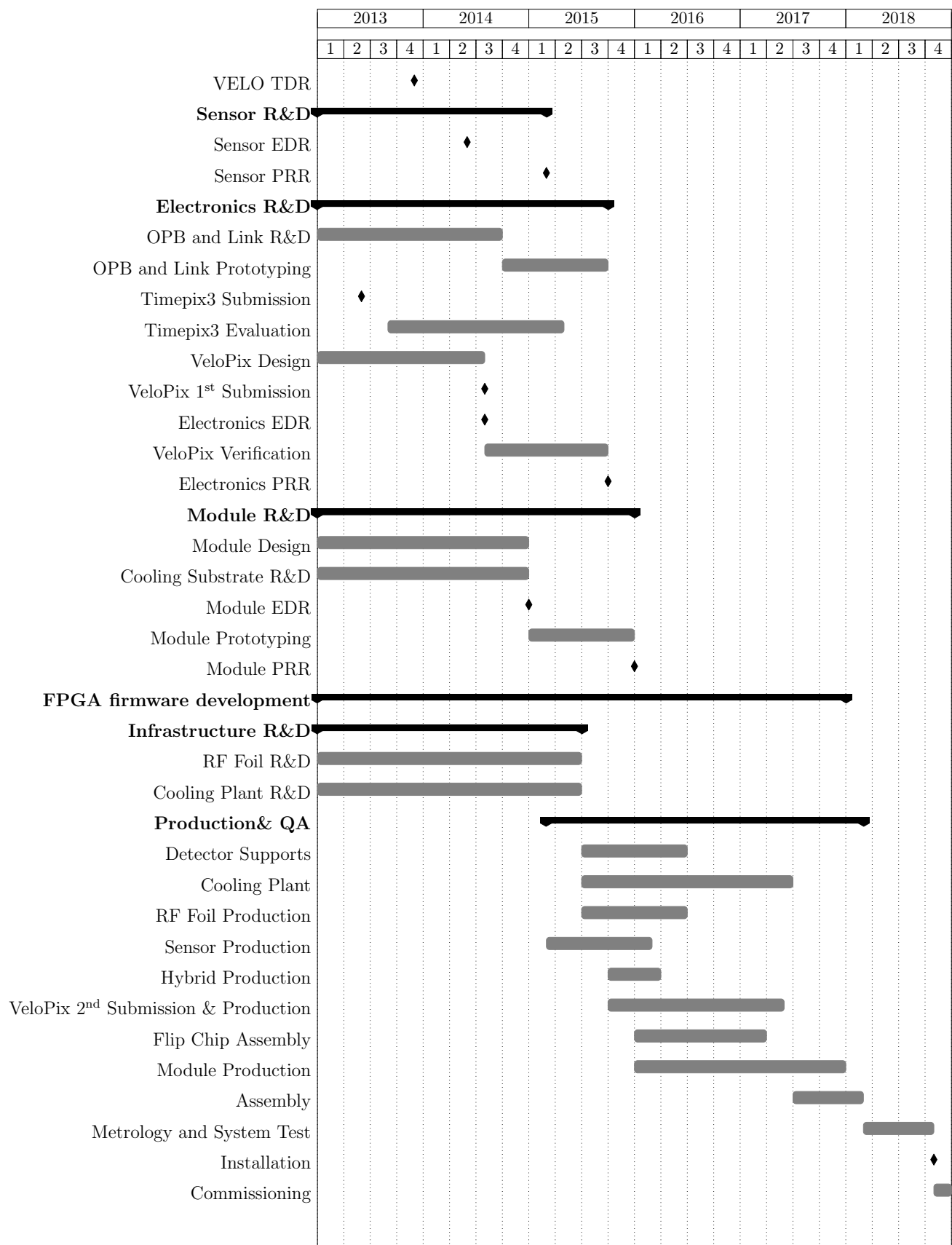


Figure 75: Project schedule for the LHCb VELO upgrade from start 2013 to end 2018. The commissioning period is expected to extend up to the end of Q2 2019.

### 11.3 Cost, resources and contingencies

The estimated VELO upgrade core cost is presented in Table 16. The estimate is based on current knowledge, including where possible quotes from industry and extrapolating from the cost of the current VELO. The assumed exchange rates of Swiss francs to other currencies are: UK pounds 1.5, Euro 1.2, US dollar 0.9.

Table 16: VELO upgrade project core costs in units of kCHF.

<b>Detector modules</b>	
Sensors	460
Front-end hybrid	113
Module cooling	403
Total	<b>976</b>
<b>Electronics</b>	
VeloPix ASIC	1598
Electrical links & feedthroughs	239
Opto and power boards	452
DAQ & ECS boards	867
General electronics	345
Total	<b>3501</b>
<b>Infrastructure</b>	
RF Foil	360
Cooling plant	270
Vacuum & motion	181
Other mechanics & cooling	505
Total	<b>1316</b>
<b>Grand total</b>	<b>5793</b>

The breakdown of cost estimates for the detector are shown in Table 17. The pixel sensor cost covers prototyping and production of the full number of sensors, plus sufficient spares to cover development steps for bump bonding, irradiation tests, beam tests, module construction and contingency. The thinning, dicing and bump bonding steps include 50% spares plus contingency. The production of module cooling substrates include 50% spares. Note that in all cases the spares include items needed for prototyping, irradiation tests, and in certain cases destruction tests. The main item of contingency to be covered is the risk of the cooling substrate manufacture failing at a chosen company, and an urgent production needed elsewhere. The potential cost of this is covered in the UK funding scheme which includes a mechanism for large contingency items.

The breakdown of cost estimates for the electronics are shown in Table 18. The cost of 15% spares are included. The cost estimates are believed to be known reasonably accurately

Table 17: VELO upgrade detector project core costs.

Item	# units	Total cost (kCHF)	Category cost (kCHF)
<b>Sensors</b>			
Pixel sensors	208	236	
Sensor thinning and dicing	208	57	
Tile bump bonding	208	167	
Total			<b>460</b>
<b>Front-end hybrid</b>			
Prototyping & test setup	1	30	
Jig development & production	1	10	
Production hybrids	104	52	
Total including 40% spares			<b>113</b>
<b>Module cooling</b>			
NRE	1	20	
Masks	6	24	
Production	52	312	
Dicing, drilling & metallisation		15	
QA		32	
Total			<b>403</b>
<b>Grand total</b>			<b>976</b>

and additional contingency is not covered here, although there is a small allowance in the UK funding scheme. We foresee two submissions in the VeloPix schedule.

The breakdown of cost estimates for the infrastructure are shown in Table 19. It is assumed that the cooling plant must undergo significant rebuild in order to cope with the additional heat dissipated in the upgraded VELO detector. Since the upgraded UT detector has similar requirements it is assumed that the cooling plant can be partially shared between the two systems. Sharing a cooling plant will result in significant savings in cost and resources, at the price of a small increase in complexity such that the plant can safely supply two independent systems. The refurbishment of the vacuum system is estimated at approximately 282 kCHF. There is an overlap between this refurbishment and the necessary long term maintenance of the VELO. For this reason the costs are partially offset from the VELO M&O budget.

The total cost estimate shows a small increase from the FTDR costs, reflecting our updated knowledge and the current status of the project and schedule.

Table 18: VELO upgrade electronics project core costs.

Item	# units	unit cost (CHF)	Total cost (kCHF)	Category cost (kCHF)
<b>VeloPix ASIC</b>				
Submission	2	480k	960	
Wafer production	48		156	
Wafer dicing & thinning	48		10	
MPW runs			72	
Electrical characterisation			180	
Specialised test equipment			220	
Total				<b>1598</b>
<b>Electrical links &amp; feedthroughs</b>				
Material per module	52	365	19	
Fabrication	520	200	104	
Connectors	624	15	9	
Feedthroughs	52	900	47	
Break-out fibres	182	160	29	
Total including 15% spares				<b>239</b>
<b>Opto and power boards</b>				
VTTx	832	200	166	
VTRx	156	150	23	
DC/DC	832	25	21	
GBTx	156	50	8	
SCA	156	30	5	
PCB	52	500+NRE	29	
Mezzanine	52	500+NRE	29	
LV & HV connectors	416	50-100	31	
Crates	8	10000	80	
Total including 15% spares				<b>452</b>
<b>DAQ &amp; ECS boards</b>				
TELL40	20	33	660	
Crates	2	10	20	
SOL40	2	37	74	
Total including 15% spares				<b>867</b>
<b>General electronics</b>				
LV system	1		120	
HV system	1		150	
Test equipment	1		75	
Total				<b>345</b>
<b>Grand total</b>				<b>3501</b>

Table 19: VELO upgrade infrastructure project core costs.

Item	Total cost (kCHF)	Category cost (kCHF)
<b>RF foil</b>		
Tooling & prototyping	72	
Production of 4 boxes	252	
Other costs	36	
Total		<b>360</b>
<b>Cooling plant</b>		
Freon system	78	
CO <sub>2</sub> system	276	
Controls	138	
Shared system	48	
Cost to VELO upgrade		<b>270</b>
<b>Vacuum &amp; motion</b>		
Vacuum pumps	145	
Valves, switches	89	
Controls	48	
After M&O offset		<b>181</b>
<b>Other mechanics and cooling</b>		
Evaporator & transfer lines	200	
Safety vacuum box	50	
Detector bases & hoods	200	
Assembly & transport	55	
Total		<b>505</b>
<b>Grand total</b>		<b>1316</b>



## 12 Acknowledgements

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